Proximity Sensor With Interrupt, IRED, and I²C Interface



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DESCRIPTION

VCNL3040 integrates a proximity sensor (PS), and a high power IRED into one small package. It incorporates photodiodes, amplifiers, and analog to digital converting circuits into a single chip by CMOS process. PS programmable interrupt features of individual high and low thresholds offers the best utilization of resource and power saving on the microcontroller.

The 12-bit / 16-bit proximity sensing function uses on intelligent cancellation scheme, so that cross talk phenomenon is eliminated effectively. To accelerate the PS response time, smart persistence prevents the misjudgment of proximity sensing but also keeps a fast response time. Active force mode, one time trigger by one instruction, is another good approach for more design flexibility to fulfill different kinds of applications with more power saving.

The VCNL3040 provides an excellent temperature compensation capability for keeping output stable under various temperature configurations. PS functions are easily operated via the simple command format of I²C (SMBus compatible) interface protocol. Operating voltage ranges from 2.5 V to 3.6 V. VCNL3040 is packaged in a lead (Pb)-free 8 pin QFN package, which offers the best market-proven reliability quality.

FEATURES

- Package type: surface-mount
- Dimensions (L x W x H in mm): 4.0 x 2.0 x 1.1
- Integrated modules: infrared emitter (IRED), proximity sensor (PS), and signal conditioning IC
- Temperature compensation: -40 °C to +85 °C
- Low power consumption I²C (SMBus compatible) interface
- Floor life: 168 h, MSL 3, according to J-STD-020
- Output type: I²C bus (PS)
- Operation voltage: 2.5 V to 3.6 V
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

e4

RoHS COMPLIANT

HALOGEN FREE

GREEN (5-2008)

PROXIMITY FUNCTION

- Immunity to red glow (940 nm IRED)
- Programmable IRED sink current
- Intelligent cancellation to reduce cross talk
- Smart persistence scheme to reduce PS response time
- Selectable for 12-bit / 16-bit PS output data

INTERRUPT

- Programmable interrupt function for PS with upper and lower thresholds
- Adjustable persistence to prevent false triggers for PS

APPLICATIONS

- Handheld device
- Consumer device
- Industrial application

PRODUCT SUMMARY

PART NUMBER	OPERATING RANGE (mm)	OPERATING VOLTAGE RANGE (V)	I²C BUS VOLTAGE RANGE (V)	IRED PULSE CURRENT (mA)	OUTPUT CODE	ADC RESOLUTION PROXIMITY / AMBIENT LIGHT
VCNL3040	0 to 300	2.5 to 3.6	1.8 to 3.6	200	12 bit / 16-bit, I²C	16 bit / n/a

ORDERING INFORMATION

ORDERING CODE	PACKAGING	VOLUME (1)	PIN NUMBER	REMARKS
VCNL3040	Tape and reel	MOQ: 2500 pcs	8	4.0 mm x 2.0 mm x 1.1 mm

Note

(1) MOQ: minimum order quantity

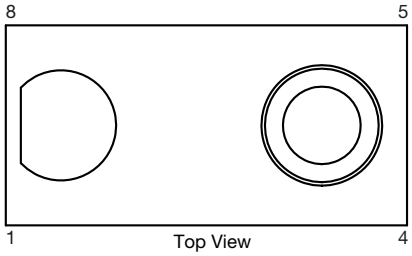
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ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)					
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**MAX.**	**UNIT**
Supply voltage		V_{DD}	2.5	3.6	V
Operation temperature range		T_{amb}	-40	+85	°C
Storage temperature range		T_{stg}	-40	+100	°C

RECOMMENDED OPERATING CONDITIONS (T_{amb} = 25 °C, unless otherwise specified)					
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**MAX.**	**UNIT**
Supply voltage		V_{DD}	2.5	3.6	V
Operation temperature range		T_{amb}	-40	+85	°C
I^2C bus operating frequency		$f_{(I2CCLK)}$	10	400	kHz

PIN DEFINITION



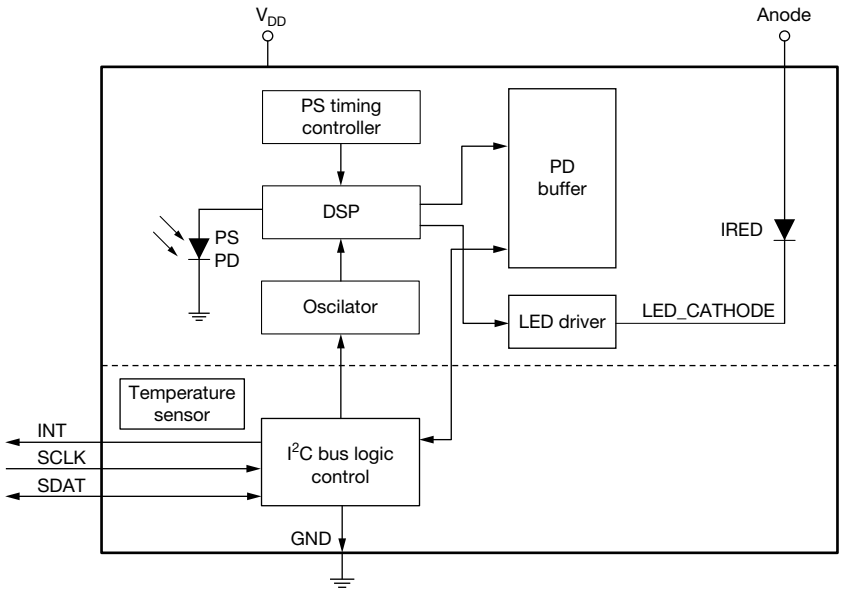
1	V_{DD}	5	Anode
2	NC	6	SCLK
3	GND	7	INT
4	Cathode	8	SDA

PIN DESCRIPTIONS			
PIN ASSIGNMENT	**SYMBOL**	**TYPE**	**FUNCTION**
1	V_{DD}	I	Power supply input
2	NC	-	No connection
3	GND	I	Ground
4	CATHODE	I	IRED cathode connection
5	ANODE	I	Anode for IRED
6	SCLK	I	I^2C digital bus clock input
7	INT	O	Interrupt pin
8	SDAT	I / O (open drain)	I^2C data bus data input / output

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BLOCK DIAGRAM



BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)							
PARAMETER		**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Supply voltage			V_{DD}	2.5	-	3.6	V
Supply current		Excluded LED driving, V_{DD} = 2.28 V	I_{DD}	-	300	-	µA
Shutdown current		Light condition = dark, V_{DD} = 3.3 V	I_{DD} (SD)	0.01	0.2	1	µA
I²C supply voltage			V_{pull_up}	1.8	-	3.6	V
I²C signal input	Logic high	V_{DD} = 3.3 V	V_{IH}	1.55	-	-	V
	Logic low		V_{IL}	-	-	0.4	
	Logic high	V_{DD} = 2.6 V	V_{IH}	1.4	-	-	V
	Logic low		V_{IL}	-	-	0.4	
Peak sensitivity wavelength of PS			λ_{pps}	-	850	-	nm
Full PS counts		12-bit / 16-bit resolution		-	-	4096 / 65 535	steps
PS dark offset		V_{DD}/V_{LED} = 2.8 V, PS_IT = 1T, IRED current = 100 mA, dark room		0	-	3	steps
PS detection range		Kodak gray card		0	-	300	mm
Operating temperature range			T_{amb}	-40	-	+85	°C
IRED driving current		(1)		-	-	200	mA

Note

(1) Programmable between 50 mA and 200 mA

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I²C BUS TIMING CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	**SYMBOL**	**STANDARD MODE**		**FAST MODE**		**UNIT**
		MIN.	**MAX.**	**MIN.**	**MAX.**	
Clock frequency	$f_{(SMBCLK)}$	10	100	10	400	kHz
Bus free time between start and stop condition	$t_{(BUF)}$	4.7	-	1.3	-	µs
Hold time after (repeated) start condition; after this period, the first clock is generated	$t_{(HDSTA)}$	4.0	-	0.6	-	µs
Repeated start condition setup time	$t_{(SUSTA)}$	4.7	-	0.6	-	µs
Stop condition setup time	$t_{(SUSTO)}$	4.0	-	0.6	-	µs
Data hold time	$t_{(HDDAT)}$	0	3450	0	900	ns
Data setup time	$t_{(SUDAT)}$	250	-	100	-	ns
I²C clock (SCK) low period	$t_{(LOW)}$	4.7	-	1.3	-	µs
I²C clock (SCK) high period	$t_{(HIGH)}$	4.0	-	0.6	-	µs
Clock / data fall time	$t_{(F)}$	-	300	-	300	ns
Clock / data rise time	$t_{(R)}$	-	1000	-	300	ns

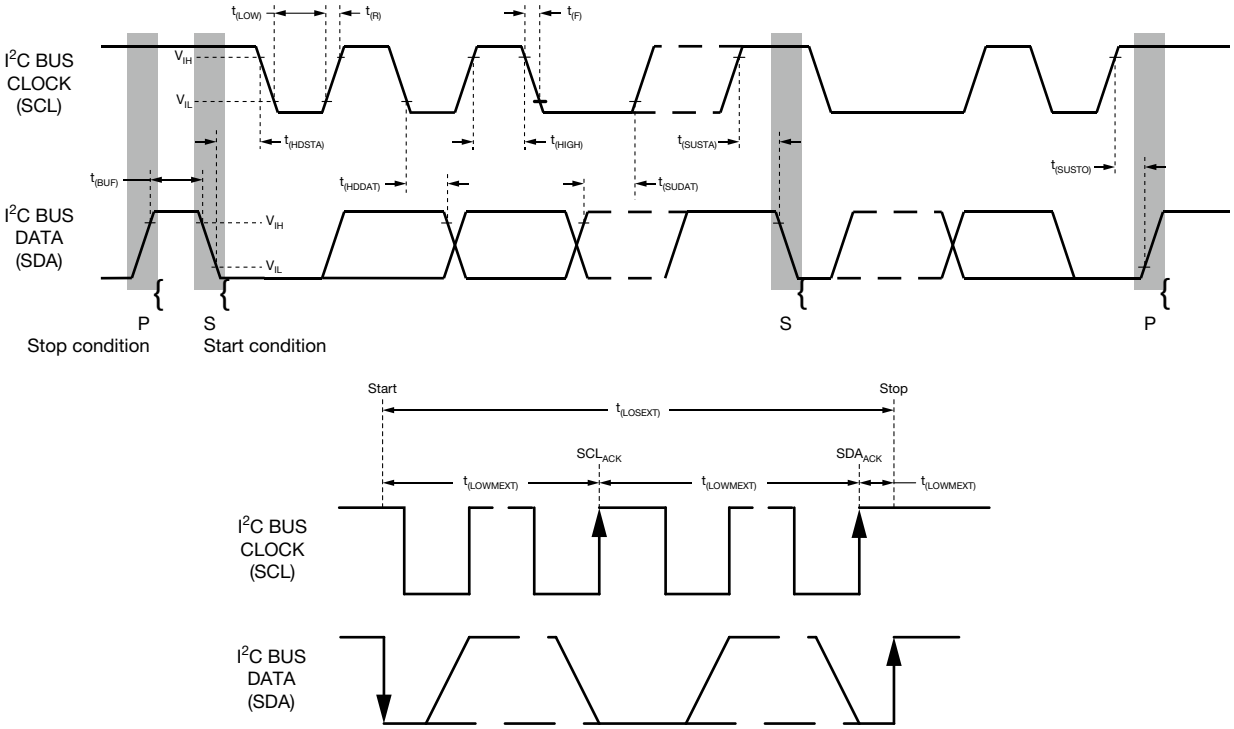


Fig. 1 - I²C Bus Timing Diagram

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PARAMETER TIMING INFORMATION

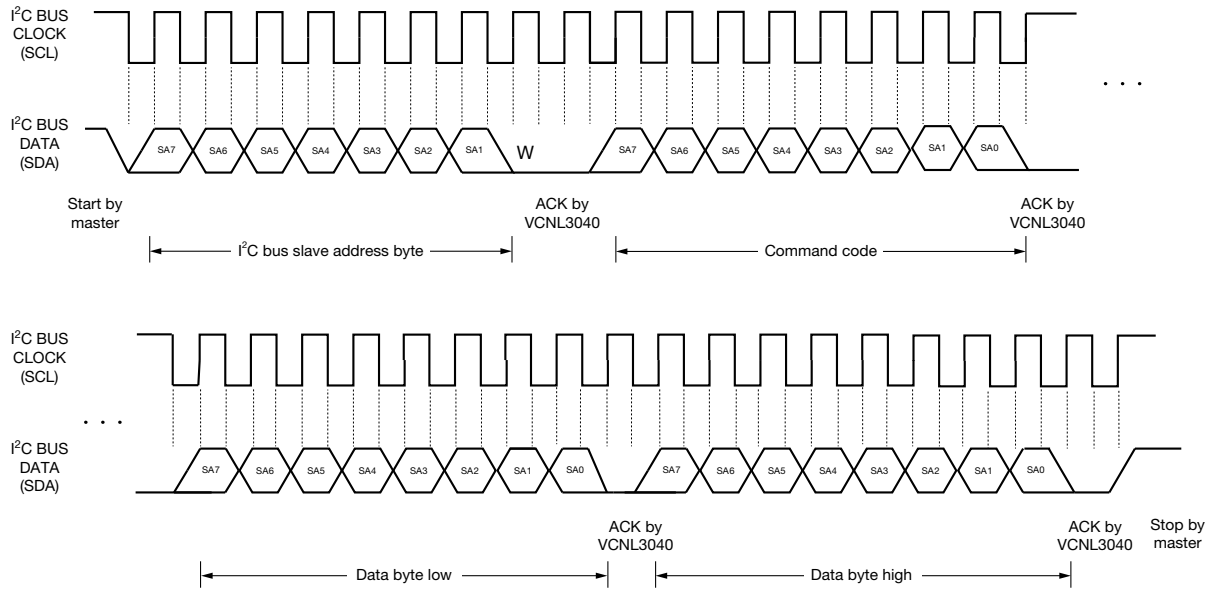


Fig. 2 - I²C Bus Timing for Sending Word Command Format

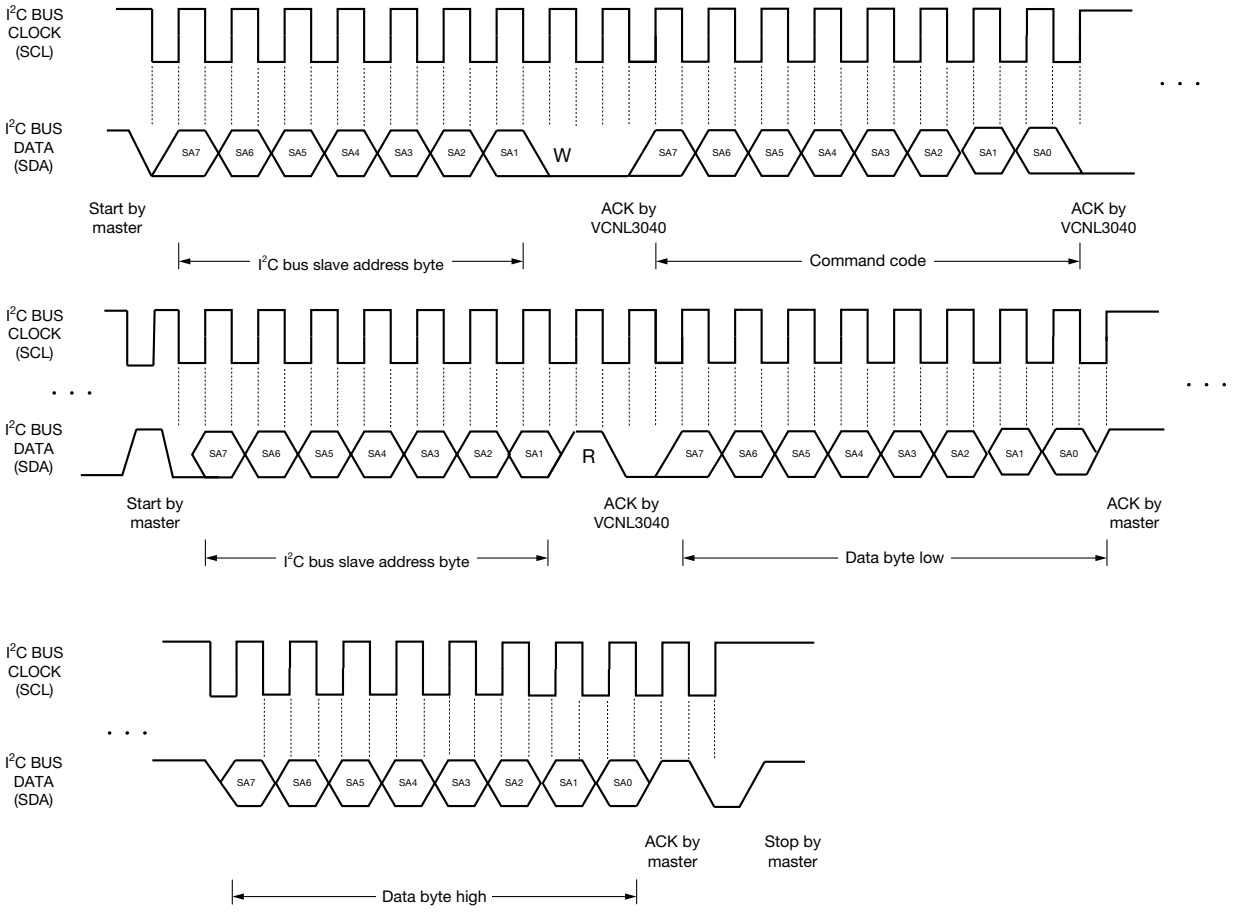


Fig. 3 - I²C Bus Timing for Receiving Word Command Format

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TYPICAL PERFORMANCE CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

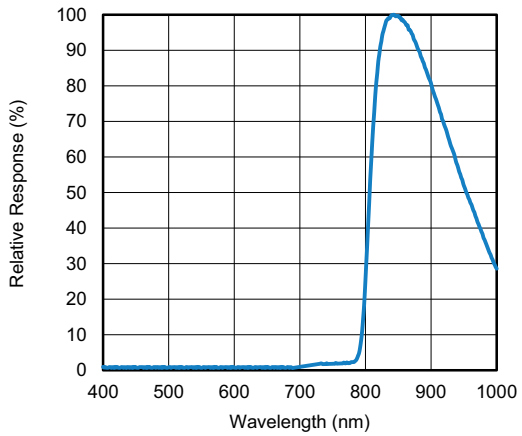


Fig. 4 - Normalized Spectral Response

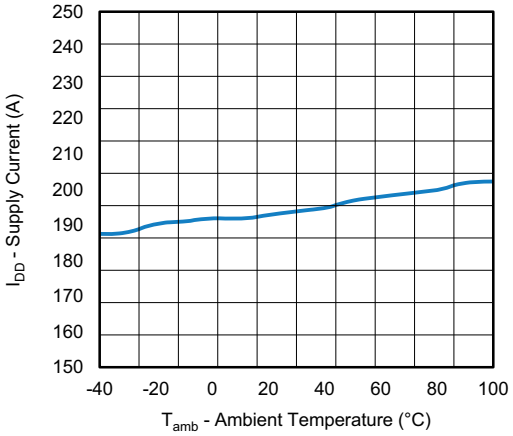


Fig. 6 - I_{DD} vs.Temperature

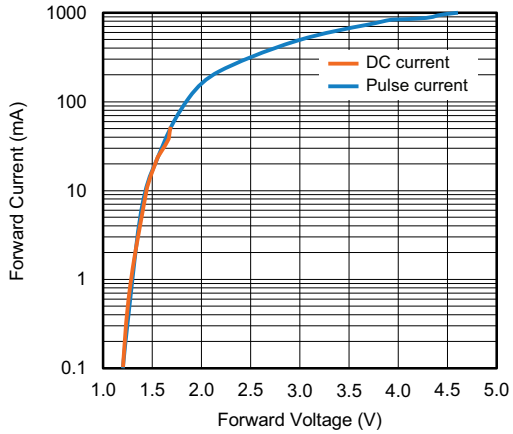
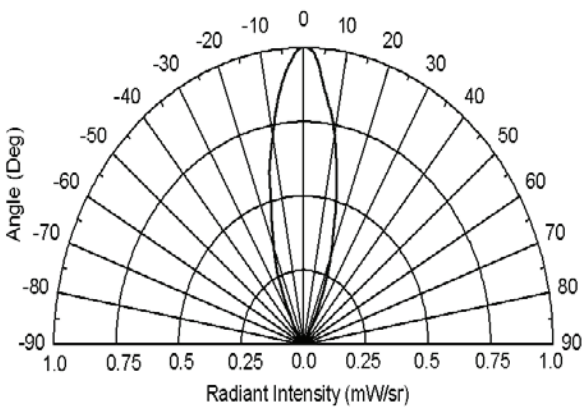


Fig. 5 - Forward Current vs. Forward Voltage



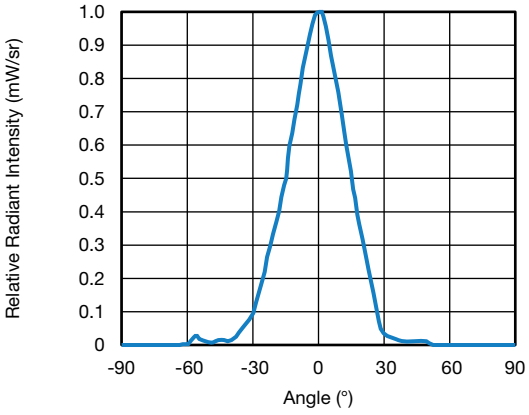


Fig. 7 - IRED Profile

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APPLICATION INFORMATION

Pin Connection with the Host

VCNL3040 integrates proximity sensor, and IRED all together with I²C interface. It is very easy for the baseband (CPU) to access PS output data via I²C interface without extra software algorithms. The hardware schematic is shown in the following diagram.

Two additional capacitors in the circuit can be used for the following purposes: (1) the 0.1 µF capacitor near the V_{DD} pin is used for power supply noise rejection, (2) the 1 µF capacitor, close to the anode pin, is used to prevent the IRED voltage from instantly dropping when the IRED is turned on, and (3) 1.5 kΩ to 2.2 kΩ is suitable for the pull up resistor of I²C except for the 10 kΩ applied on the INT pin.

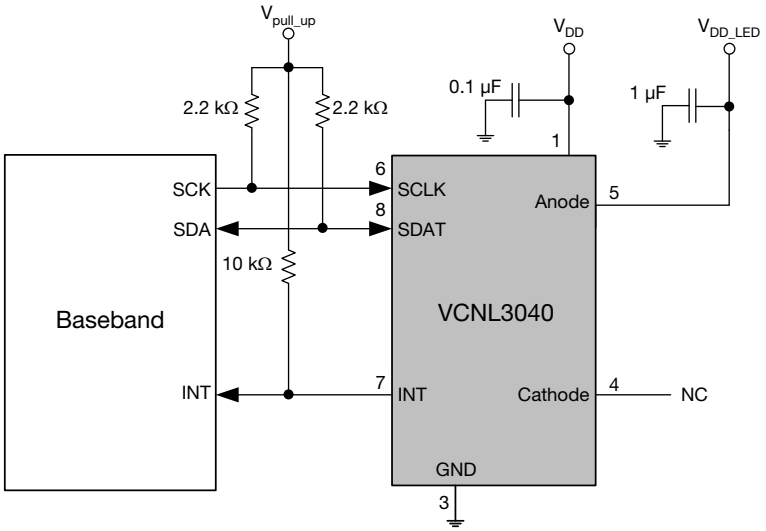


Fig. 8 - Hardware Pin Connection Diagram

Digital Interface

VCNL3040 applies single slave address 0x60 (HEX) of 7-bit addressing following I²C protocol. All operations can be controlled by the command register. The simple command structure helps users easily program the operation setting and latch the light data from VCNL3040. As Fig. 9 shows, VCNL3040's I²C command format is simple for read and write operations between VCNL3040 and the host. The white sections indicate host activity and the gray sections indicate VCNL3040's acknowledgement of the host access activity. Write word and read word protocol is suitable for accessing registers particularly for 12-bit / 16-bit PS data. Interrupt can be cleared by reading data out from register: INT_Flag. All command codes should follow read word and write word protocols.



Fig. 9 - Write Word and Read Word Protocol

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Function Description

VCNL3040 supports different kinds of mechanical designs to achieve the best proximity detection performance for any color of object with more flexibility. The basic PS function settings, such as duty ratio, integration time, interrupt, and PS enable / disable and persistence, are handled by the register: PS_CONF1. Duty ratio controls the PS response time. Integration time represents the duration of the energy being received. The Interrupt is asserted when the PS detection levels over the high threshold level setting (register: PS_THDH) or lower than low threshold (register: PS_THDL). If the Interrupt function is enabled, the host reads the PS output data from VCNL3040 that saves host loading from periodically reading PS data. Additionally, the INT flag (register: INT_Flag) indicates the behavior of INT triggered under different conditions. PS persistence (PS_PERS) sets up the PS INT asserted conditions as long as the PS output value continually exceeds the threshold level. The intelligent cancellation level can be set on register: PS_CANC to reduce the cross talk phenomenon.

VCNL3040 also supports an easy use of proximity detection logic output mode that outputs just high / low levels saving loading from the host. Normal operation mode or proximity detection logic output mode can be selected on the register: PS_MS. A smart persistence is provided to get faster PS response time and prevent false trigger for PS. Descriptions of each slave address operation are shown in table 1.

TABLE 1 - COMMAND CODE AND REGISTER DESCRIPTION

COMMAND CODE	DATE BYTE LOW / HIGH	REGISTER NAME	R / W	DEFAULT VALUE	FUNCTION DESCRIPTION
0x00	L	Reserved	R / W	0x01	Reserved
	H	Reserved	-	0x00	Reserved
0x01	L	Reserved	-	0x00	Reserved
	H	Reserved	-	0x00	Reserved
0x02	L	Reserved	-	0x00	Reserved
	H	Reserved	-	0x00	Reserved
0x03	L	PS_CONF1	R/W	0x03	PS duty ratio, integration time, persistence, and PS enable/disable
	H	PS_CONF2	R/W	0x00	PS gain, PS output resolution selection, PS interrupt trigger method
0x04	L	PS_CONF3	R/W	0x00	PS multi pulse, active force mode, sunlight immunity setting
	H	PS_MS	R/W	0x00	PS mode selection, PS protection setting and IRED current selection
0x05	L	PS_CANC_L	R/W	0x00	PS cancellation level setting
	H	PS_CANC_M	R/W	0x00	PS cancellation level setting
0x06	L	PS_THDL_L	R/W	0x00	PS low interrupt threshold setting LSB byte
	H	PS_THDL_M	R/W	0x00	PS low interrupt threshold setting MSB byte
0x07	L	PS_THDH_L	R/W	0x00	PS high interrupt threshold setting LSB byte
	H	PS_THDH_M	R/W	0x00	PS high interrupt threshold setting MSB byte
0x08	L	PS_Data_L	R	0x00	PS LSB output data
	H	PS_Data_M	R	0x00	PS MSB output data
0x09	L	Reserved	-	0x00	Reserved
	H	Reserved	-	0x00	Reserved
0x0A	L	Reserved	-	0x00	Reserved
	H	Reserved	-	0x00	Reserved
0x0B	L	Reserved	-	0x00	Reserved
	H	INT_Flag	R	0x00	PS interrupt flags
0x0C	L	ID_L	R	0x86	Device ID LSB
	H	ID_M	R	0x01	Device ID MSB

Note

- All of the reserved registers are used for internal test, please keep as default setting

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Command Register Format

VCNL3040 provides an 8-bit command register for PS controlling independently. The description of each command format is shown in following tables.

TABLE 2 - REGISTER: 00H_L DESCRIPTION

REGISTER NAME		COMMAND CODE: 0x00_L (0x00 DATA BYTE LOW)
Command	Bit	Description
Reserved	7 : 0	Default = (0 : 0 : 0 : 0 : 0 : 0 : 0 : 0)

TABLE 3 - REGISTER: 00H_H DESCRIPTION

Reserved		COMMAND CODE: 0x00_H (0x00 DATA BYTE HIGH)
Command	Bit	Description
Reserved	7 : 0	Default = (0 : 0 : 0 : 0 : 0 : 0 : 0 : 0)

TABLE 4 - REGISTER: PS_CONF1 DESCRIPTION

PS_CONF1		COMMAND CODE: 0x03_L (0x03 DATA BYTE LOW)
Command	Bit	Description
PS_Duty	7 : 6	(0 : 0) = 1/40, (0 : 1) = 1/80, (1 : 0) = 1/160, (1 : 1) = 1/320 PS IRED on / off duty ratio setting
PS_PERS	5 : 4	(0 : 0) = 1, (0 : 1) = 2, (1 : 0) = 3, (1 : 1) = 4 PS interrupt persistence setting
PS_ IT	3 : 1	(0 : 0 : 0) = 1T, (0 : 0 : 1) = 1.5T, (0 : 1 : 0) = 2T, (0 : 1 : 1) = 2.5T, (1 : 0 : 0) = 3T, (1 : 0 : 1) = 3.5T, (1 : 1 : 0) = 4T, (1 : 1 : 1) = 8T, PS integration time setting
PS_SD	0	0 = PS power on, 1 = PS shut down, default = 1

TABLE 5 - REGISTER: PS_CONF2 DESCRIPTION

PS_CONF2		COMMAND CODE: 0x03_H (0x03 DATA BYTE HIGH)
Command	Bit	Description
Reserved	7 : 6	(0 : 0), reserved
Reserved	5 : 4	(0 : 0), reserved
PS_HD	3	0 = PS output is 12 bits, 1 = PS output is 16 bits
Reserved	2	Default = 0
PS_INT	1 : 0	(0 : 0) = interrupt disable, (0 : 1) = trigger by closing, (1 : 0) = trigger by away, (1 : 1) = trigger by closing and away

TABLE 6 - REGISTER: PS_CONF3 DESCRIPTION

PS_CONF3		COMMAND CODE: 0x04_L (0x04 DATA BYTE LOW)
Command	Bit	Description
Reserved	7	Default = 0
Reserved	6 : 5	(0 : 0)
PS_SMART_PERS	4	0 = disable; 1 = enable PS smart persistence
PS_FOR	3	0 = active force mode disable (normal mode), 1 = active force mode enable
PS_FOR_TRIG	2	0 = no PS active force mode trigger, 1 = trigger one time cycle The VCNL3040 conducts a single measurement every time the host writes a “1” to this bit. The state returns to “0” automatically
Reserved	1 : 0	(0 : 0)

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TABLE 7 - REGISTER: PS_MS DESCRIPTION		
PS_MS		**COMMAND CODE: 0x04_H (0x04 DATA BYTE HIGH)**
Command	Bit	Description
Reserved	7	Reserved
PS_MS	6	0 = normal interrupt functionality, 1 = proximity detection logic output mode enable
Reserved	5 : 3	(0 : 0 : 0)
LED_I	2 : 0	(0 : 0 : 0) = 50 mA, (0 : 0 : 1) = 75 mA, (0 : 1 : 0) = 100 mA, (0 : 1 : 1) = 120 mA, (1 : 0 : 0) = 140 mA, (1 : 0 : 1) = 160 mA, (1 : 1 : 0) = 180 mA, (1 : 1 : 1) = 200 mA LED current selection setting

TABLE 8 - REGISTER: PS_CANC_L AND PS_CANC_M DESCRIPTION		
PS_CANC_L PS_CANC_M		**COMMAND CODE: 0x05_L (0x05 DATA BYTE LOW) AND 0x05_H (0x05 DATA BYTE HIGH)**
Register	Bit	Description
PS_CANC_L	7 : 0	0x00 to 0xFF, PS cancellation level setting, LSB byte
PS_CANC_M	7 : 0	0x00 to 0xFF, PS cancellation level setting, MSB byte

TABLE 9 - REGISTER: PS_THDL_L AND PS_THDL_M DESCRIPTION		
PS_THDL_L PS_THDL_M		**COMMAND CODE: 0x06_L (0x06 DATA BYTE LOW) AND 0x06_H (0x06 DATA BYTE HIGH)**
Register	Bit	Description
PS_THDL_L	7 : 0	0x00 to 0xFF, PS low interrupt threshold setting, LSB byte
PS_THDL_M	7 : 0	0x00 to 0xFF, PS low interrupt threshold setting, MSB byte

TABLE 10 - REGISTER: PS_THDH_L AND PS_THDH_M DESCRIPTION		
PS_THDH_L PS_THDH_M		**COMMAND CODE: 0x07_L (0x07 DATA BYTE LOW) AND 0x07_H (0x07 DATA BYTE HIGH)**
Register	Bit	Description
PS_THDH_L	7 : 0	0x00 to 0xFF, PS high interrupt threshold setting, LSB byte
PS_THDH_M	7 : 0	0x00 to 0xFF, PS high interrupt threshold setting, MSB byte

TABLE 11 - READ OUT REGISTER DESCRIPTION			
REGISTER	**COMMAND CODE**	**BIT**	**DESCRIPTION**
PS_Data_L	0x08_L (0x08 data byte low)	7 : 0	0x00 to 0xFF, PS LSB output data
PS_Data_M	0x08_H (0x08 data byte high)	7 : 0	0x00 to 0xFF, PS MSB output data
Reserved	0x09_L (0x09 data byte low)	7 : 0	Reserved
Reserved	0x09_H (0x09 data byte high)	7 : 0	Reserved
Reserved	0x0A_L (0x0A data byte low)	7 : 0	Reserved
Reserved	0x0A_H (0x0A data byte high)	7 : 0	Reserved
Reserved	0x0B_L (0x0B data byte low)	7 : 0	Default = 0x00
INT_Flag	0x0B_H (0x0B data byte high)	7 6 5 4 3 2 1 0	Reserved PS_SPFLAG, PS entering protection mode Reserved Reserved Reserved Reserved PS_IF_CLOSE, PS rises above PS_THDH INT trigger event PS_IF_AWAY, PS drops below PS_THDL INT trigger event
ID_L	0CH_L (0CH data byte low)	7 : 0	86H for MP version sample device ID LSB byte
ID_M	0CH_H (0CH data byte high)	7 : 6 5 : 4 3 : 0	(0 : 0) (0 : 0) slave address = 0x60 (7-bit) version code (0 : 0 : 0 : 1) Device ID MSB byte

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Adjustable Sampling Time

VCNL3040's embedded LED driver, drives the internal IRED with the "LED_CATHODE" pin by a pulsed duty cycle. The IRED on / off duty ratio is programmable by I^2C command at register: PS_Duty allows the user to adjust the current consumption and PS response time. The higher the duty ratio set, the faster response time achieved with higher power consumption. For example, PS_Duty = 1/320, peak IRED current = 100 mA, the average current consumption is 100 mA/320 = 0.3125 mA.

Initialization

The VCNL3040 includes default values for each register. As long as power is on, it is ready to be controlled by host via I^2C bus.

Threshold Window Setting

- Programmable PS Threshold

  VCNL3040 provides both high and low thresholds 16-bit data setting for PS.(Register: PS_THDL, PS_THDH)

- PS Persistence

  The PS persistence function (PS_PERS, 1\2\3\4) helps to avoid false trigger of the PS INT. For example, if PS_PERS = 3 times, the PS INT will not be asserted unless the PS value is greater than the PS threshold (PS_THDH) value for three consecutive measurements

- PS Active Force Mode

  An extreme power saving way to use PS is to apply PS active force (register: PS_CONF3 command: PS_FOR = 1) mode. Anytime host would like to read out just one of PS data, write in "1" at register: PS_CONF3 command: PS_FOR_Trig. Without commands placed, there is no PS data output. VCNL3040 stays in standby mode constantly

Intelligent Cancellation

The VCNL3040 provides an intelligent cancellation method to reduce cross talk phenomenon for the proximity sensor. The output data is subtracted by the input value on register: PS_CANC.

Interruption (INT)

The VCNL3040 has PS interrupt feature operated by a single pin "INT". The purpose of the interrupt feature is to actively inform the host once INT has been asserted. With the interrupt function applied, the host does not need to be constantly polling data from the sensor, but to read data from the sensor while receiving interrupt request from the sensor. As long as the host enables PS interrupt (register: PS_INT) function, the level of INT pin (pin 7) is pulled low once INT asserted. All registers are accessible even if INT is asserted. To effectively adopt PS INT function, it is recommended to use Vishay PS detection mechanism at register: PS_INT = 1 for the best PS detection performance which can be adjusted by high / low THD level of PS. PS INT trigger type is defined by register: PS_INT.

Interruption Flag

The register: INT_Flag represents all of interrupt trigger status for PS. When flag value changes from "0" to "1" state, the level of INT pin will be pulled low. When the host reads INT_Flag data, the bit will change from "1" state to "0" state after reading out, the INT level will be returned to high afterwards.

PROXIMITY DETECTION LOGIC OUTPUT MODE

The VCNL3040 provides a proximity detection logic output mode that uses INT pin (pin 7) as a proximity detection logic high / low output (register: PS_MS). When this mode is selected, the PS output (pin 7; INT/P_{OUT}) is pulled low when an object is closing to be detected and returned to level high when the object moves away. Register: PS_THDH\L defines how sensitive PS detection is.

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PROXIMITY DETECTION HYSTERESIS

A hysteresis is created by setting the low and high threshold values. With proximity detection logic mode disabled, an interrupt event will trigger and stay triggered until it is cleared in the INT_Flag register. The register is cleared automatically once it is read. If the interrupt flags are not cleared after an interrupt event has occurred, the VCNL3040 will not react to another interrupt event until the INT-Flag register has been cleared. An example of this could be when turning on and off a backlight of a mobile display. First the PS INT triggers when the PS value is over PS_THDH. The host switches off the panel backlight and then clears INT. When PS value is less than PS_THDL, host switches on panel backlight.

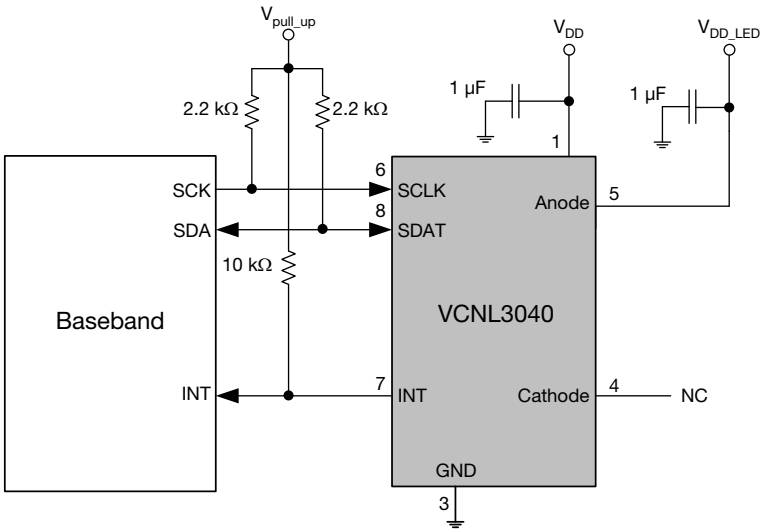
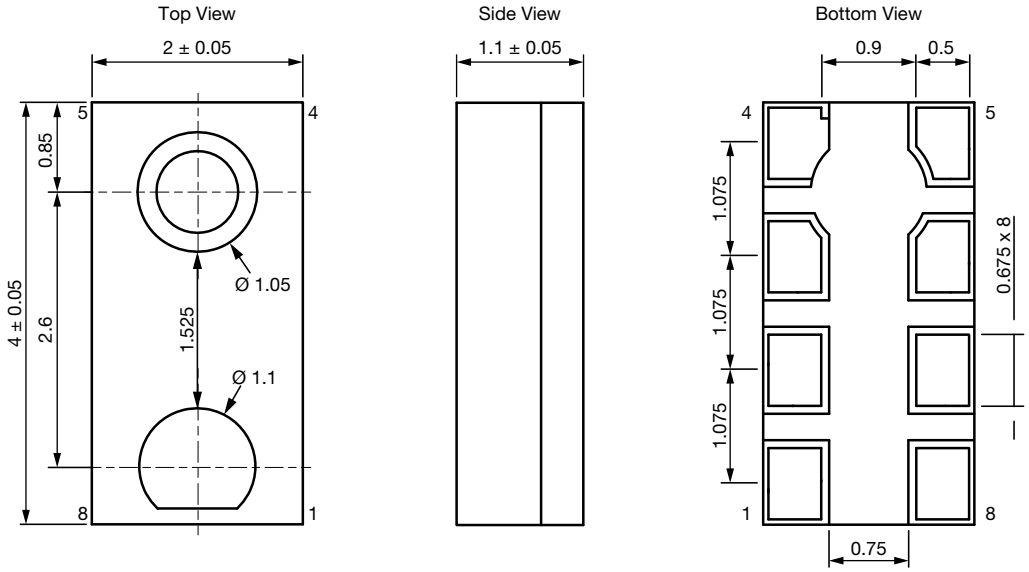


Fig. 10 - VCNL3040 Reference Circuit Connection With Host (proximity detection logic output mode)
(VCNL3040 INT pin connecting to BB GPIO instead of INT pin)

PACKAGE INFORMATION in millimeters



1	V_{DD}	5	Anode
2	NC	6	SCLK
3	GND	7	INT
4	Cathode	8	SDA

Fig. 11 - VCNL3040 Package Dimensions

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LAYOUT NOTICE AND REFERENCE CIRCUIT in millimeters

Pad and Circuit Layout Reference

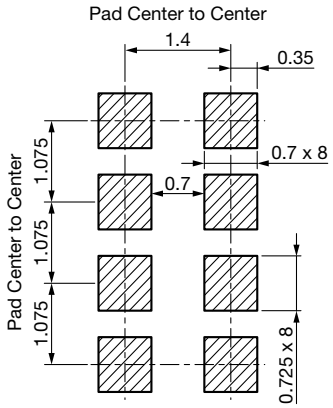


Fig. 12 - VCNL3040 PCB Layout Footprint

APPLICATION CIRCUIT BLOCK REFERENCE

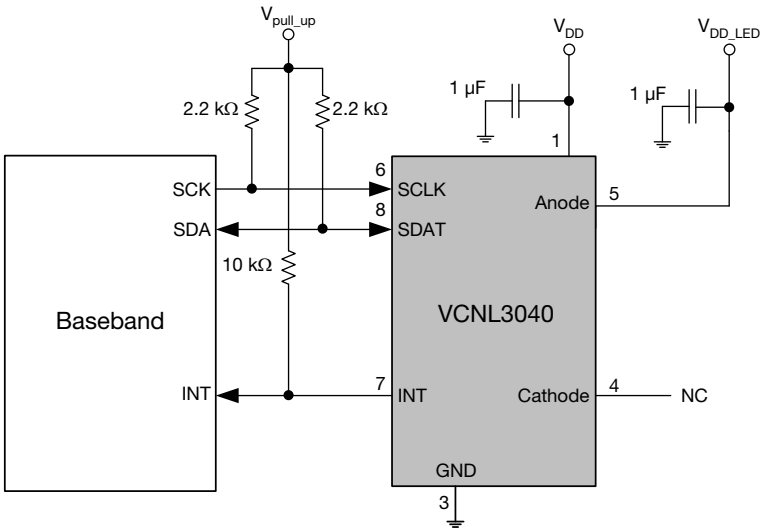


Fig. 13 - VCNL3040 Application Circuit

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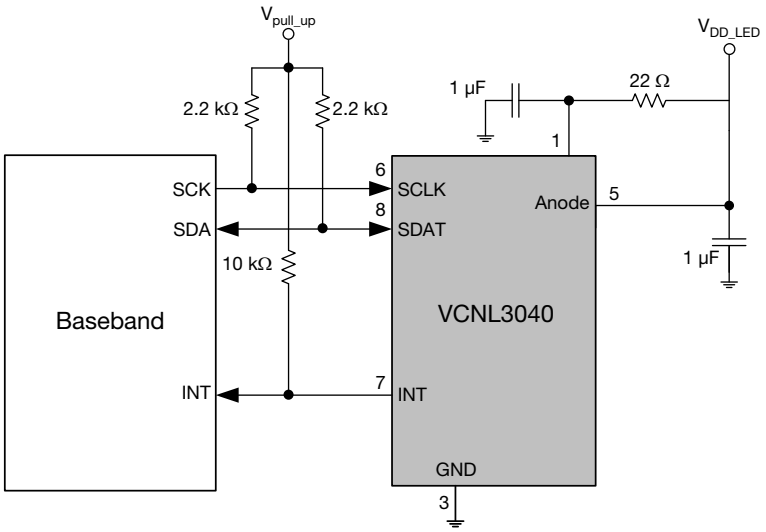


Fig. 14 - VCNL3040 Application Circuit
V_{DD} (sensor and LED connected together) Suggestion Circuit

RECOMMENDED STORAGE AND REBAKING CONDITIONS				
PARAMETER	**CONDITIONS**	**MIN.**	**MAX.**	**UNIT**
Storage temperature		-40	+85	°C
Relative humidity		-	60	%
Open time		-	168	h
Total time	From the date code on the aluminized envelope (unopened)	-	12	months
Rebaking	Tape and reel: 60 °C	-	22	h
	Tube: 60 °C	-	22	h

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RECOMMENDED INFRARED REFLOW

Soldering conditions which are based on J-STD-020 C.

IR REFLOW PROFILE CONDITION			
PARAMETER	**CONDITIONS**	**TEMPERATURE**	**TIME**
Peak temperature		260 °C + 5 °C / - 5 °C (max.: 265 °C)	10 s
Preheat temperature range and timing		150 °C to 200 °C	60 s to 180 s
Timing within 5 °C to peak temperature			10 s to 30 s
Timing maintained above temperature / time		217 °C	60 s to 150 s
Timing from 25 °C to peak temperature			8 min (max.)
Ramp-up rate		3 °C/s (max.)	
Ramp-down rate		6 °C/s (max.)	

Recommend Normal Solder Reflow is 235 °C to 255 °C.

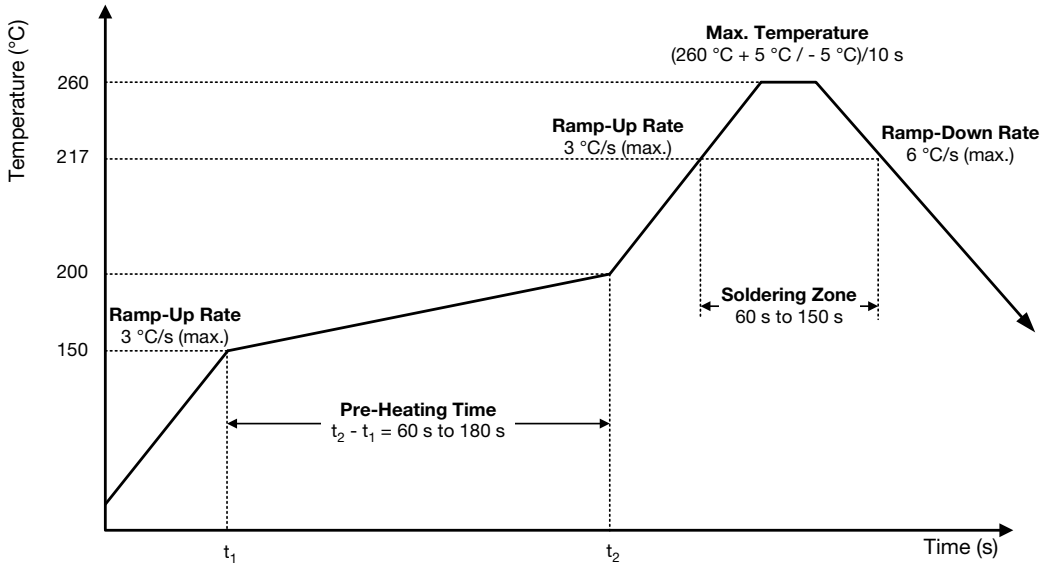


Fig. 15 - VCNL3040 Solder Reflow Profile Chart

RECOMMENDED IRON TIP SOLDERING CONDITION AND WARNING HANDLING

1. Solder the device with the following conditions:
   1.1. Soldering temperature: 400 °C (max.)
   1.2. Soldering time: 3 s (max.)
2. If the temperature of the method portion rises in addition to the residual stress between the leads, the possibility that an open or short circuit occurs due to the deformation or destruction of the resin increases
3. The following methods: VPS and wave soldering, have not been suggested for the component assembly
4. Cleaning method conditions:
   4.1. Solvent: methyl alcohol, ethyl alcohol, isopropyl alcohol
   4.2. Solvent temperature < 45 °C (max.)
   4.3. Time: 3 min (min.)

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TAPE PACKAGING INFORMATION in millimeters

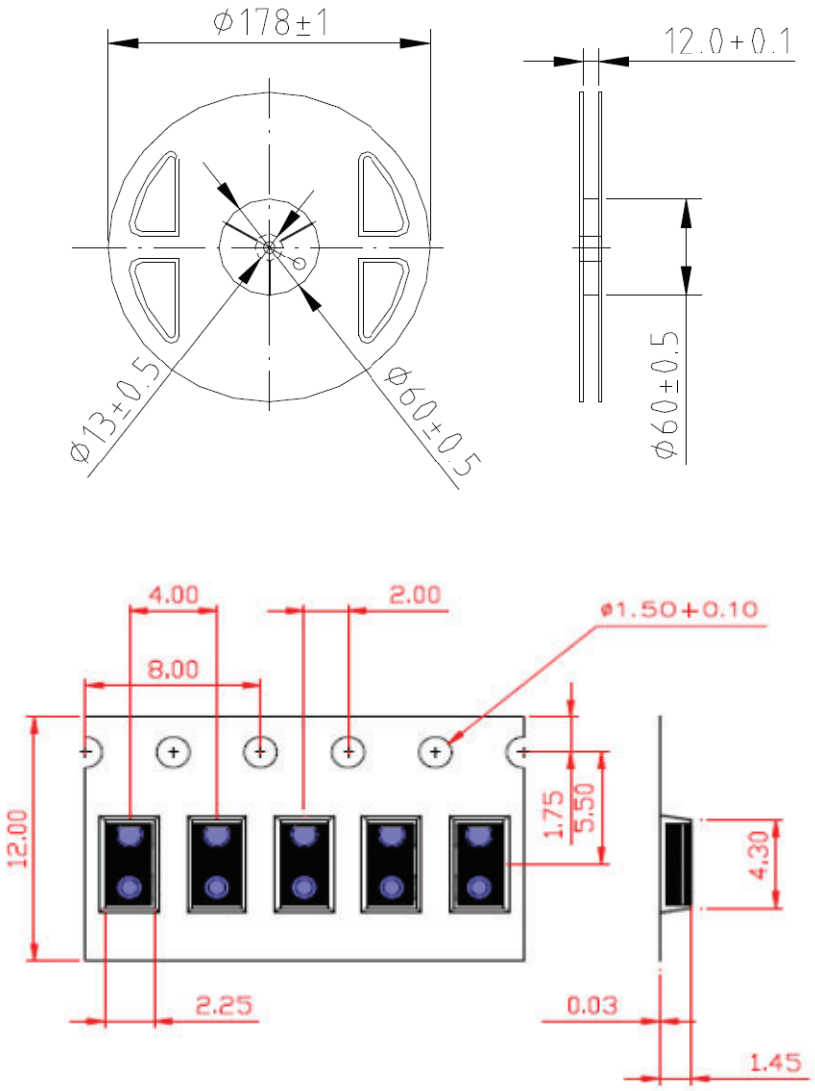


Fig. 16 - Reel Dimensions

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