CY7C1444KV33
CY7C1445KV33

36-Mbit (1M × 36/2M × 18) Pipelined DCD Sync SRAM

Features

- Supports bus operation up to 250 MHz
- Available speed grades is 250 MHz
- Registered inputs and outputs for pipelined operation
- Optimal for performance (double-cycle deselect)
- Depth expansion without wait state
- 3.3-V core power supply
- 2.5-V or 3.3-V I/O power supply
- Fast clock-to-output times
  - 2.5 ns (for 250-MHz device)
- Provide high-performance 3-1-1-1 access rate
- User-selectable burst counter supporting interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed writes
- Asynchronous output enable
- CY7C1444KV33, CY7C1445KV33 available in JEDEC-standard Pb-free 100-pin TQFP packages
- "ZZ" sleep mode option

Functional Description

The CY7C1444KV33/CY7C1445KV33 SRAMs integrate 1M × 36/2M × 18 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock (CLK) input. The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable ($\overline{CE}_1$), depth-expansion chip enables (CE_2 and $\overline{CE}_3$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), write enables ($\overline{BW}_X$, and $\overline{BWE}$), and global write ($\overline{GW}$). Asynchronous inputs include the output enable ($\overline{OE}$) and the ZZ pin.

Addresses and chip enables are registered at rising edge of clock when either address strobe processor ($\overline{ADSP}$) or address strobe controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as controlled by the advance pin ($\overline{ADV}$).
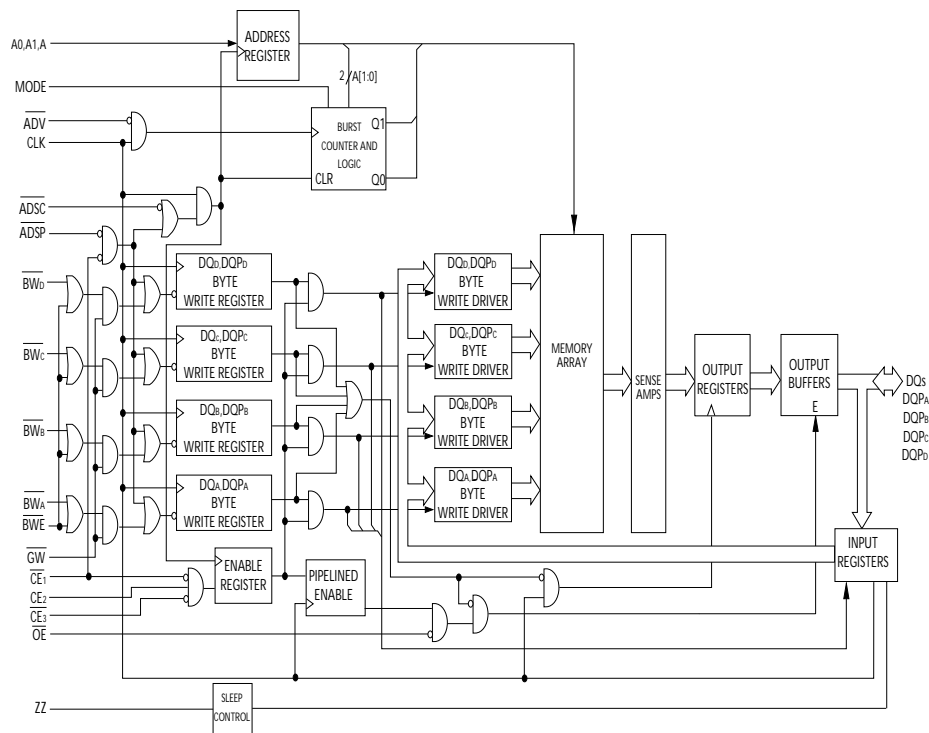
Address, data inputs, and write controls are registered on-chip to initiate a self-timed write cycle. This part supports byte write operations (see Pin Descriptions and Truth Table for further details). Write cycles can be one to four bytes wide as controlled by the byte write control inputs. $\overline{GW}$ active LOW causes all bytes to be written. This device incorporates an additional pipelined enable register which delays turning off the output buffers an additional cycle when a deselect is executed. This feature allows depth expansion without penalizing system performance.

The CY7C1444KV33/CY7C1445KV33 SRAMs operate from a +3.3 V core power supply while all outputs operate with a +3.3 V or a +2.5 V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.
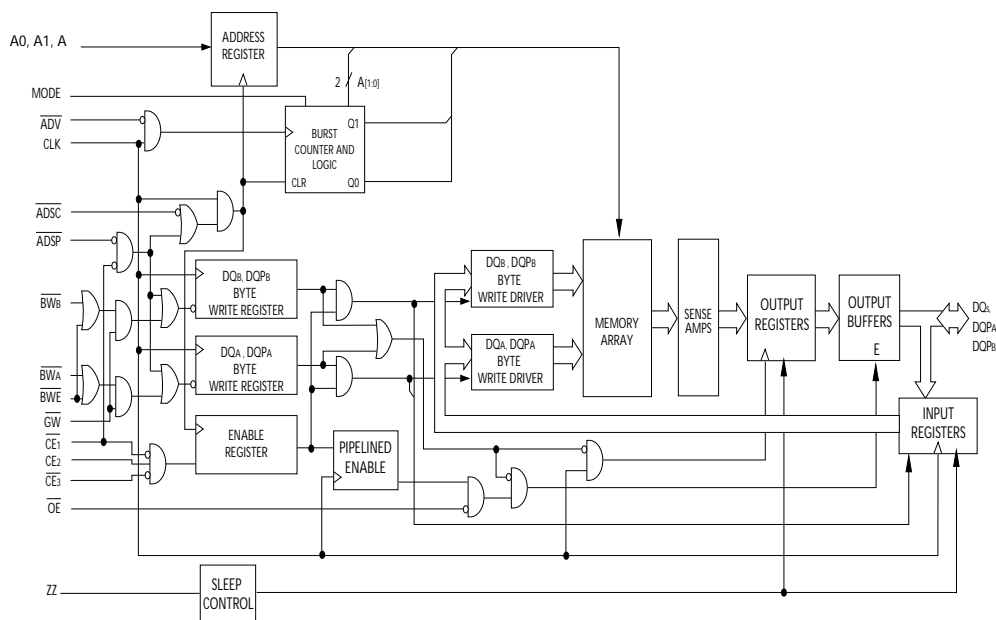
Selection Guide

Description		250 MHz	Unit
Maximum access time		2.5	ns
Maximum operating current	× 18	220	mA
	× 36	240	

Logic Block Diagram – CY7C1444KV33

Logic Block Diagram – CY7C1445KV33

Contents

Pin Configurations

Figure 1. 100-pin TQFP Pinout

CY7C1444KV33 (1M × 36)

Top edge (pins 100–81): A, A, $\overline{CE_1}$, CE_2, $\overline{BW_D}$, $\overline{BW_C}$, $\overline{BW_B}$, $\overline{BW_A}$, CE_3, V_{DD}, V_{SS}, CLK, $\overline{GW}$, $\overline{BWE}$, $\overline{OE}$, $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$, A, A

Left side (pins 1–30):
1 DQP$_C$
2 DQ$_C$
3 DQ$_C$
4 V$_{DDQ}$
5 V$_{SSQ}$
6 DQ$_C$
7 DQ$_C$
8 DQ$_C$
9 DQ$_C$
10 V$_{SSQ}$
11 V$_{DDQ}$
12 DQ$_C$
13 DQ$_C$
14 NC
15 V$_{DD}$
16 NC
17 V$_{SS}$
18 DQ$_D$
19 DQ$_D$
20 V$_{DDQ}$
21 V$_{SSQ}$
22 DQ$_D$
23 DQ$_D$
24 DQ$_D$
25 DQ$_D$
26 V$_{SSQ}$
27 V$_{DDQ}$
28 DQ$_D$
29 DQ$_D$
30 DQP$_D$

Right side (pins 80–51):
80 DQP$_B$
79 DQ$_B$
78 DQ$_B$
77 V$_{DDQ}$
76 V$_{SSQ}$
75 DQ$_B$
74 DQ$_B$
73 DQ$_B$
72 DQ$_B$
71 V$_{SSQ}$
70 V$_{DDQ}$
69 DQ$_B$
68 DQ$_B$
67 V$_{SS}$
66 NC
65 V$_{DD}$
64 ZZ
63 DQ$_A$
62 DQ$_A$
61 V$_{DDQ}$
60 V$_{SSQ}$
59 DQ$_A$
58 DQ$_A$
57 DQ$_A$
56 DQ$_A$
55 V$_{SSQ}$
54 V$_{DDQ}$
53 DQ$_A$
52 DQ$_A$
51 DQP$_A$

Bottom edge (pins 31–50): MODE, A, A, A, A_1, A_0, NC/72M, A, V$_{SS}$, V$_{DD}$, A, A, A, A, A, A, A, A, A, A

CY7C1445KV33 (2M × 18)

Top edge (pins 100–81): A, A, $\overline{CE_1}$, CE_2, NC, NC, $\overline{BW_B}$, $\overline{BW_A}$, CE_3, V_{DD}, V_{SS}, CLK, $\overline{GW}$, $\overline{BWE}$, $\overline{OE}$, $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$, A, A

Left side (pins 1–30):
1 NC
2 NC
3 NC
4 V$_{DDQ}$
5 V$_{SSQ}$
6 NC
7 NC
8 DQ$_B$
9 DQ$_B$
10 V$_{SSQ}$
11 V$_{DDQ}$
12 DQ$_B$
13 DQ$_B$
14 NC
15 V$_{DD}$
16 NC
17 V$_{SS}$
18 DQ$_B$
19 DQ$_B$
20 V$_{DDQ}$
21 V$_{SSQ}$
22 DQ$_B$
23 DQ$_B$
24 DQP$_B$
25 NC
26 V$_{SSQ}$
27 V$_{DDQ}$
28 NC
29 NC
30 NC

Right side (pins 80–51):
80 A
79 NC
78 NC
77 V$_{DDQ}$
76 V$_{SSQ}$
75 NC
74 DQP$_A$
73 DQ$_A$
72 DQ$_A$
71 V$_{SSQ}$
70 V$_{DDQ}$
69 DQ$_A$
68 DQ$_A$
67 V$_{SS}$
66 NC
65 V$_{DD}$
64 ZZ
63 DQ$_A$
62 DQ$_A$
61 V$_{DDQ}$
60 V$_{SSQ}$
59 DQ$_A$
58 DQ$_A$
57 NC
56 NC
55 V$_{SSQ}$
54 V$_{DDQ}$
53 NC
52 NC
51 NC

Bottom edge (pins 31–50): MODE, A, A, A, A_1, A_0, NC/72M, A, V$_{SS}$, V$_{DD}$, A, A, A, A, A, A, A, A, A, A

Pin Definitions

Name	I/O	Description
A_0, A_1, A	Input-synchronous	**Address inputs used to select one of the address locations**. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are sampled active. A1: A0 are fed to the two-bit counter..
$\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$	Input-synchronous	**Byte write select inputs, active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-synchronous	**Global write enable input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (all bytes are written, regardless of the values on BW_X and BWE).
$\overline{BWE}$	Input-synchronous	**Byte write enable input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-clock	**Clock input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
$\overline{CE_1}$	Input-synchronous	**Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE_3}$ to select/deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH. $\overline{CE_1}$ is sampled only when a new external address is loaded.
CE_2	Input-synchronous	**Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $\overline{CE_3}$ to select/deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE_3}$	Input-synchronous	**Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and CE_2 to select/deselect the device. $\overline{CE_3}$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-asynchronous	**Output enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, DQ pins are tristated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	Input-synchronous	**Advance input signal, sampled on the rising edge of CLK, active LOW**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-synchronous	**Address strobe from processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1: A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. ASDP is ignored when $\overline{CE_1}$ is deasserted HIGH.
$\overline{ADSC}$	Input-synchronous	**Address strobe from controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1: A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
ZZ	Input-asynchronous	**ZZ "sleep" input, active HIGH**. When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQs, DQPs	I/O-synchronous	**Bidirectional data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQP_X are placed in a tristate condition.
V_{DD}	Power supply	**Power supply inputs to the core of the device**.
V_{SS}	Ground	**Ground for the core of the device**.
V_{SSQ}	I/O ground	**Ground for the I/O circuitry**.

Pin Definitions (continued)

Name	I/O	Description
V_{DDQ}	I/O power supply	**Power supply for the I/O circuitry**.
MODE	Input-static	**Selects burst order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode pin has an internal pull-up.
NC	–	**No Connects**. Not internally connected to the die.
NC/72M, NC/144M, NC/288M, NC/576M, NC/1G	–	**No Connects**. Not internally connected to the die. 72M, 144M, 288M, 576M, and 1G are address expansion pins are not internally connected to the die.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock.

The CY7C1444KV33/CY7C1445KV33 support secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium processors. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the processor address strobe (ADSP) or the controller address strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the byte write enable (BWE) and byte write select (BW_X) inputs. A global write enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Synchronous chip selects CE_1, CE_2, CE_3 and an asynchronous output enable (OE) provide for easy bank selection and output tristate control. ADSP is ignored if CE_1 is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) ADSP or ADSC is asserted LOW, (2) chip selects are all asserted active, and (3) the write signals (GW, BWE) are all deasserted HIGH. ADSP is ignored if CE_1 is HIGH. The address presented to the address inputs is stored into the address advancement logic and the address register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the output registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within t_{CO} if OE is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always tristated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the OE signal. Consecutive single read cycles are supported.

The CY7C1444KV33/CY7C1445KV33 are double-cycle deselect part. Once the SRAM is deselected at clock rise by the chip select and either ADSP or ADSC signals, its output will tristate immediately after the next clock rise.

Single Write Accesses Initiated by ADSP

This access is initiated when both of the following conditions are satisfied at clock rise: (1) ADSP is asserted LOW, and (2) chip select is asserted active. The address presented is loaded into the address register and the address advancement logic while being delivered to the memory core. The write signals (GW, BWE, and BW_X) and ADV inputs are ignored during this first cycle.

ADSP triggered write accesses require two clock cycles to complete. If GW is asserted LOW on the second clock rise, the data presented to the DQ_X inputs is written into the corresponding address location in the memory core. If GW is HIGH, then the write operation is controlled by BWE and BW_X signals. The CY7C1444KV33/CY7C1445KV33 provide byte write capability that is described in the Write Cycle Description table. Asserting the byte write enable input (BWE) with the selected byte write input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY7C1444KV33/CY7C1445KV33 are common I/O devices, the output enable (OE) must be deasserted HIGH before presenting data to the DQ inputs. Doing so will tristate the output drivers. As a safety precaution, DQ are automatically tristated whenever a write cycle is detected, regardless of the state of OE.

Single Write Accesses Initiated by ADSC

ADSC write accesses are initiated when the following conditions are satisfied: (1) ADSC is asserted LOW, (2) ADSP is deasserted HIGH, (3) chip select is asserted active, and (4) the appropriate combination of the write inputs (GW, BWE, and BW_X) are asserted active to conduct a write to the desired byte(s). ADSC triggered write accesses require a single clock cycle to complete. The address presented is loaded into the address register and the address advancement logic while being delivered to the memory core. The ADV input is ignored during this cycle. If a global write is conducted, the data presented to the DQ_X is written into the corresponding address location in the memory core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY7C1444KV33/CY7C1445KV33 are common I/O devices, the output enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQ_X inputs. Doing so will tristate the output drivers. As a safety precaution, DQ_X are automatically tristated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1444KV33/CY7C1445KV33 provide a two-bit wraparound counter, fed by $A_{[1:0]}$, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The burst sequence is user selectable through the MODE input. Both read and write burst operations are supported.

Asserting $\overline{ADV}$ LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode. $\overline{CE}$s, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2$ V	–	75	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2$ V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2$ V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ inactive to exit sleep current	This parameter is sampled	0	–	ns

Truth Table

The Truth Table for CY7C1444KV33/CY7C1445KV33 is as follows. [1, 2, 3, 4, 5, 6]

Operation	Add. Used	$\overline{CE}_1$	CE_2	$\overline{CE}_3$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect cycle, power-down	None	H	X	X	L	X	L	X	X	X	L–H	Tristate
Deselect cycle, power-down	None	L	L	X	L	L	X	X	X	X	L–H	Tristate
Deselect cycle, power-down	None	L	X	H	L	L	X	X	X	X	L–H	Tristate
Deselect cycle, power-down	None	L	L	X	L	H	L	X	X	X	L–H	Tristate
Deselect cycle, power-down	None	L	X	H	L	H	L	X	X	X	L–H	Tristate
Sleep mode, power-down	None	X	X	X	H	X	X	X	X	X	X	Tristate
Read cycle, begin burst	External	L	H	L	L	L	X	X	X	L	L–H	Q
Read cycle, begin burst	External	L	H	L	L	L	X	X	X	H	L–H	Tristate
Write cycle, begin burst	External	L	H	L	L	H	L	X	L	X	L–H	D
Read cycle, begin burst	External	L	H	L	L	H	L	X	H	L	L–H	Q
Read cycle, begin burst	External	L	H	L	L	H	L	X	H	H	L–H	Tristate
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	L	L–H	Q
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	H	L–H	Tristate
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	L	L–H	Q
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	H	L–H	Tristate
Write cycle, continue burst	Next	X	X	X	L	H	H	L	L	X	L–H	D
Write cycle, continue burst	Next	H	X	X	L	X	H	L	L	X	L–H	D
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	L	L–H	Q
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	H	L–H	Tristate
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	L	L–H	Q
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	H	L–H	Tristate
Write cycle, suspend burst	Current	X	X	X	L	H	H	H	L	X	L–H	D
Write cycle, suspend burst	Current	H	X	X	L	X	H	H	L	X	L–H	D

Notes
1. $\underline{X}$ = "Don't Care." H = Logic HIGH, L = Logic LOW.
2. $\overline{WRITE}$ = L when any one or more byte write enable signals and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all byte write enable signals, $\overline{BWE}$, $\overline{GW}$ = H.
3. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
4. $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are available only in the TQFP package.
5. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW}_X$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tristate. $\overline{OE}$ is a don't care for the remainder of the write cycle.
6. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tristate when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Partial Truth Table for Read/Write

The Partial Truth Table for Read/Write for CY7C1444KV33 is as follows [7, 8].

Function (CY7C1444KV33)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_D$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write byte A – (DQ$_A$ and DQP$_A$)	H	L	H	H	H	L
Write byte B – (DQ$_B$ and DQP$_B$)	H	L	H	H	L	H
Write bytes B, A	H	L	H	H	L	L
Write byte C – (DQ$_C$ and DQP$_C$)	H	L	H	L	H	H
Write bytes C, A	H	L	H	L	H	L
Write bytes C, B	H	L	H	L	L	H
Write bytes C, B, A	H	L	H	L	L	L
Write byte D – (DQ$_D$ and DQP$_D$)	H	L	L	H	H	H
Write bytes D, A	H	L	L	H	H	L
Write bytes D, B	H	L	L	H	L	H
Write bytes D, B, A	H	L	L	H	L	L
Write bytes D, C	H	L	L	L	H	H
Write bytes D, C, A	H	L	L	L	H	L
Write bytes D, C, B	H	L	L	L	L	H
Write all bytes	H	L	L	L	L	L
Write all bytes	L	X	X	X	X	X

Partial Truth Table for Read/Write

The Partial Truth Table for Read/Write for CY7C1445KV33 is as follows [7, 8].

Function (CY7C1445KV33)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	H	X	X
Read	H	L	H	H
Write byte A – (DQ$_A$ and DQP$_A$)	H	L	H	L
Write byte B – (DQ$_B$ and DQP$_B$)	H	L	L	H
Write all bytes	H	L	L	L
Write all bytes	L	X	X	X

Notes
7. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
8. Table only lists a partial listing of the byte write combinations. Any Combination of $\overline{BW}_X$ is valid Appropriate write will be done based on which byte write is active.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with
power applied .... –55 °C to +125 °C

Supply voltage on
V_{DD} relative to GND ....–0.5 V to +4.6 V

Supply voltage on
V_{DDQ} relative to GND .... –0.5 V to +V_{DD}

DC voltage applied to outputs
in tristate ....–0.5 V to V_{DDQ} + 0.5 V

DC input voltage .... –0.5 V to V_{DD} + 0.5 V

Current into outputs (LOW) .... 20 mA

Static discharge voltage
(per MIL-STD-883, method 3015) .... > 2001 V

Latch-up current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical Single-Bit Upsets	25 °C	<5	5	FIT/Mb
LMBU	Logical Multi-Bit Upsets	25 °C	0	0.01	FIT/Mb
SEL	Single Event Latch up	85 °C	0	0.1	FIT/Dev

* *No LMBU or SEL events occurred during testing*; this column represents a statistical χ^2, 95% confidence limit calculation. For more details refer to Application Note AN 54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates"

Electrical Characteristics

Over the Operating Range

Parameter [9, 10]	Description	Test Conditions	Min	Max	Unit
V_{DD}	Power supply voltage	–	3.135	3.6	V
V_{DDQ}	I/O supply voltage	for 3.3 V I/O	3.135	V_{DD}	V
		for 2.5 V I/O	2.375	2.625	V
V_{OH}	Output HIGH voltage	for 3.3 V I/O, I_{OH} = –4.0 mA	2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA	2.0	–	V
V_{OL}	Output LOW voltage	for 3.3 V I/O, I_{OL} = 8.0 mA	–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA	–	0.4	V
V_{IH}	Input HIGH voltage[9]	for 3.3 V I/O	2.0	V_{DD} + 0.3 V	V
		for 2.5 V I/O	1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW voltage[9]	for 3.3 V I/O	–0.3	0.8	V
		for 2.5 V I/O	–0.3	0.7	V
I_X	Input leakage current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}	–5	5	µA
	Input current of MODE	Input = V_{SS}	–30	–	µA
		Input = V_{DD}	–	5	µA
	Input current of ZZ	Input = V_{SS}	–5	–	µA
		Input = V_{DD}	–	30	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{DDQ}, output disabled	–5	5	µA

Notes
9. Overshoot: $V_{IH}(AC) < V_{DD} + 1.5$ V (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL}(AC) > -2$ V (Pulse width less than $t_{CYC}/2$).
10. $T_{Power-up}$: Assumes a linear ramp from 0 V to V_{DD}(min) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.

Electrical Characteristics *(continued)*

Over the Operating Range

Parameter [9, 10]	Description	Test Conditions			Min	Max	Unit
I_{DD}	V_{DD} operating supply current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	4-ns cycle, 250 MHz	× 18	–	220	mA
				× 36	–	240	
I_{SB1}	Automatic CE power-down current – TTL inputs	V_{DD} = Max, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX} = 1/t_{CYC}	4-ns cycle, 250 MHz	× 18	–	85	mA
				× 36	–	90	
I_{SB2}	Automatic CE power-down current – CMOS inputs	V_{DD} = Max, device deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ}$ – 0.3 V, f = 0	4-ns cycle, 250 MHz	× 18	–	75	mA
				× 36		80	
I_{SB3}	Automatic CE power-down current – CMOS inputs	V_{DD} = Max, device deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ}$ – 0.3 V, f = f_{MAX} = 1/t_{CYC}	4-ns cycle, 250 MHz	× 18	–	85	mA
				× 36		90	
I_{SB4}	Automatic CE power-down current – TTL inputs	V_{DD} = Max, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0	4-ns cycle, 250 MHz	×18	–	75	mA
				×36	–	80	

Capacitance

Parameter [11]	Description	Test Conditions	100-pin TQFP Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	5	pF
C_{CLK}	Clock input capacitance		5	pF
$C_{I/O}$	Input/Output capacitance		5	pF

Thermal Resistance

Parameter [11]	Description	Test Conditions		100-pin TQFP Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	With Still Air (0 m/s)	35.36	°C/W
			With Air Flow (1 m/s)	31.30	°C/W
			With Air Flow (3 m/s)	28.86	°C/W
Θ_{JC}	Thermal resistance (junction to case)		–	7.52	°C/W
Θ_{JB}	Thermal resistance (junction to board)			28.89	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms

3.3 V I/O Test Load
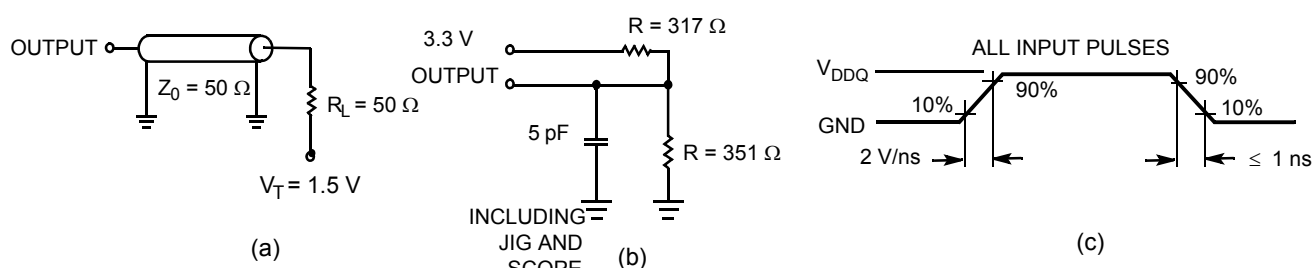
2.5 V I/O Test Load
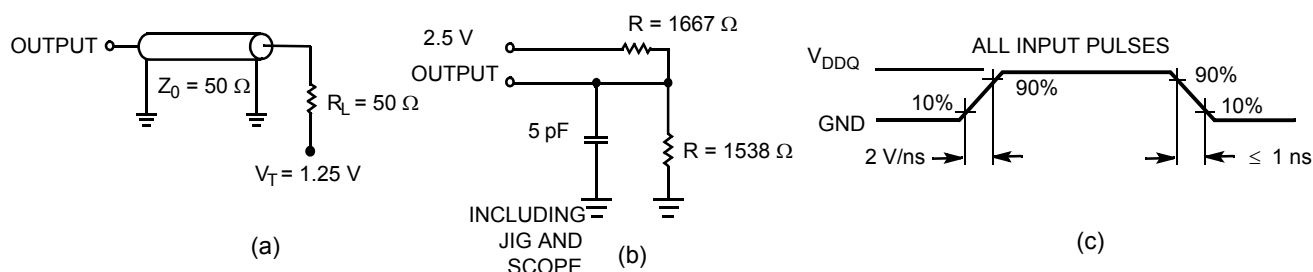
Note
11. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

Over the Operating Range

Parameter [12, 13]	Description	-250		Unit
		Min	Max	
t_{POWER}	V_{DD}(Typical) to the first access[14]	1	–	ms
Clock				
t_{CYC}	Clock cycle time	4.0	–	ns
t_{CH}	Clock HIGH	1.5	–	ns
t_{CL}	Clock LOW	1.5	–	ns
Output Times				
t_{CO}	Data output valid after CLK rise	–	2.5	ns
t_{DOH}	Data output hold after CLK rise	1.0	–	ns
t_{CLZ}	Clock to low Z[15, 16, 17]	1.0	–	ns
t_{CHZ}	Clock to high Z[15, 16, 17]	–	2.6	ns
t_{OEV}	$\overline{OE}$ LOW to output valid	–	2.6	ns
t_{OELZ}	$\overline{OE}$ LOW to output low Z[15, 16, 17]	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to output high Z[15, 16, 17]	–	2.6	ns
Set-up Times				
t_{AS}	Address set-up before CLK rise	1.2	–	ns
t_{ADS}	$\overline{ADSC}$, $\overline{ADSP}$ set-up before CLK rise	1.2	–	ns
t_{ADVS}	$\overline{ADV}$ set-up before CLK rise	1.2	–	ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ set-up before CLK rise	1.2	–	ns
t_{DS}	Data input set-up before CLK rise	1.2	–	ns
t_{CES}	Chip Enable set-up before CLK rise	1.2	–	ns
Hold Times				
t_{AH}	Address hold after CLK rise	0.3	–	ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ hold after CLK rise	0.3	–	ns
t_{ADVH}	$\overline{ADV}$ hold after CLK rise	0.3	–	ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ hold after CLK rise	0.3	–	ns
t_{DH}	Data input hold after CLK rise	0.3	–	ns
t_{CEH}	Chip Enable hold after CLK rise	0.3	–	ns

Notes
12. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
13. Test conditions shown in (a) of AC Test Loads unless otherwise noted.
14. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above $V_{DD(minimum)}$ initially before a read or write operation can be initiated.
15. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 2 on page 12. Transition is measured ± 200 mV from steady-state voltage.
16. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.
17. This parameter is sampled and not 100% tested.

Switching Waveforms

Figure 3. Read Cycle Timing [18]


DON'T CARE   UNDEFINED
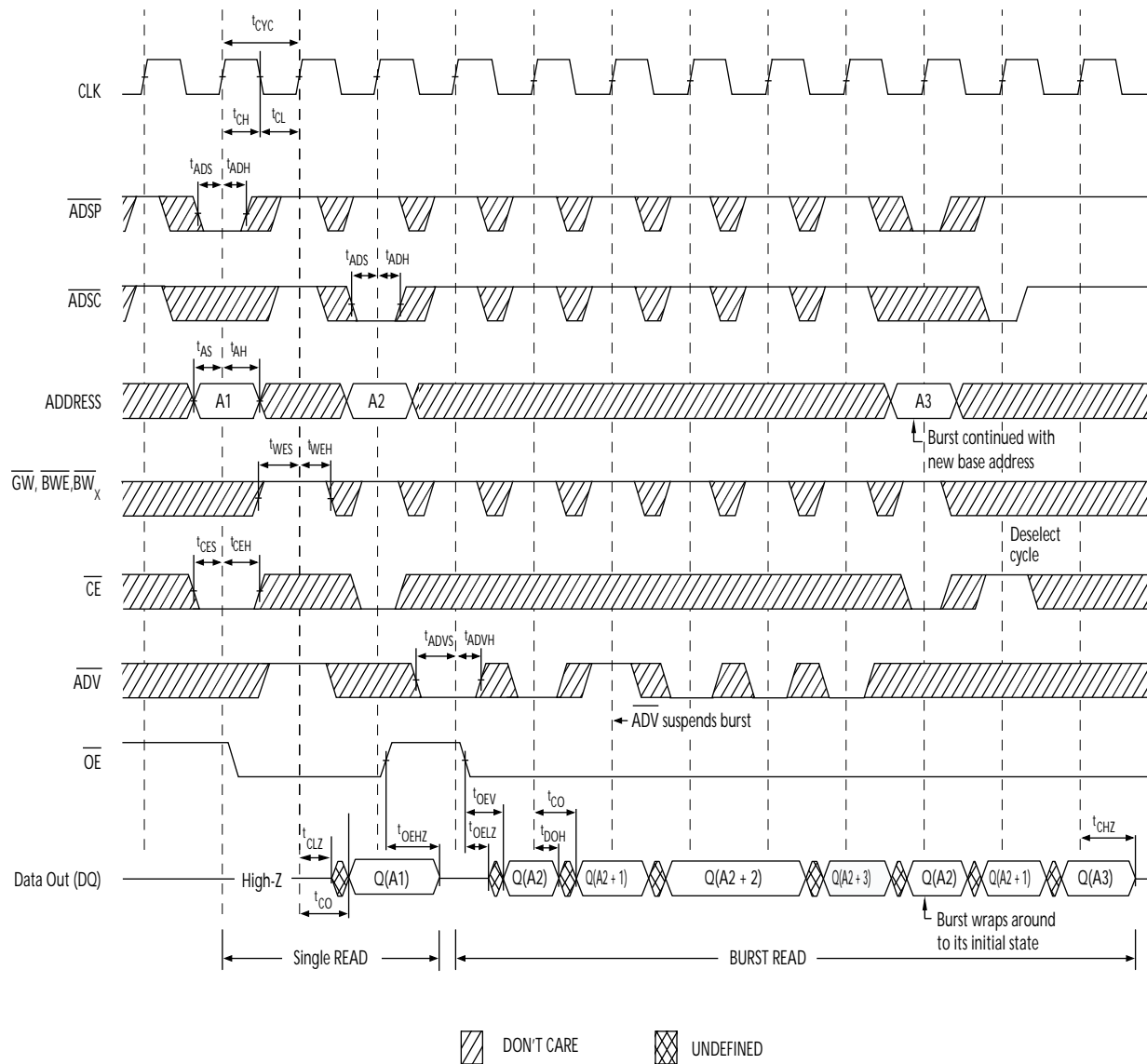
Note
18. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

Switching Waveforms *(continued)*

Figure 4. Write Cycle Timing [19, 20]
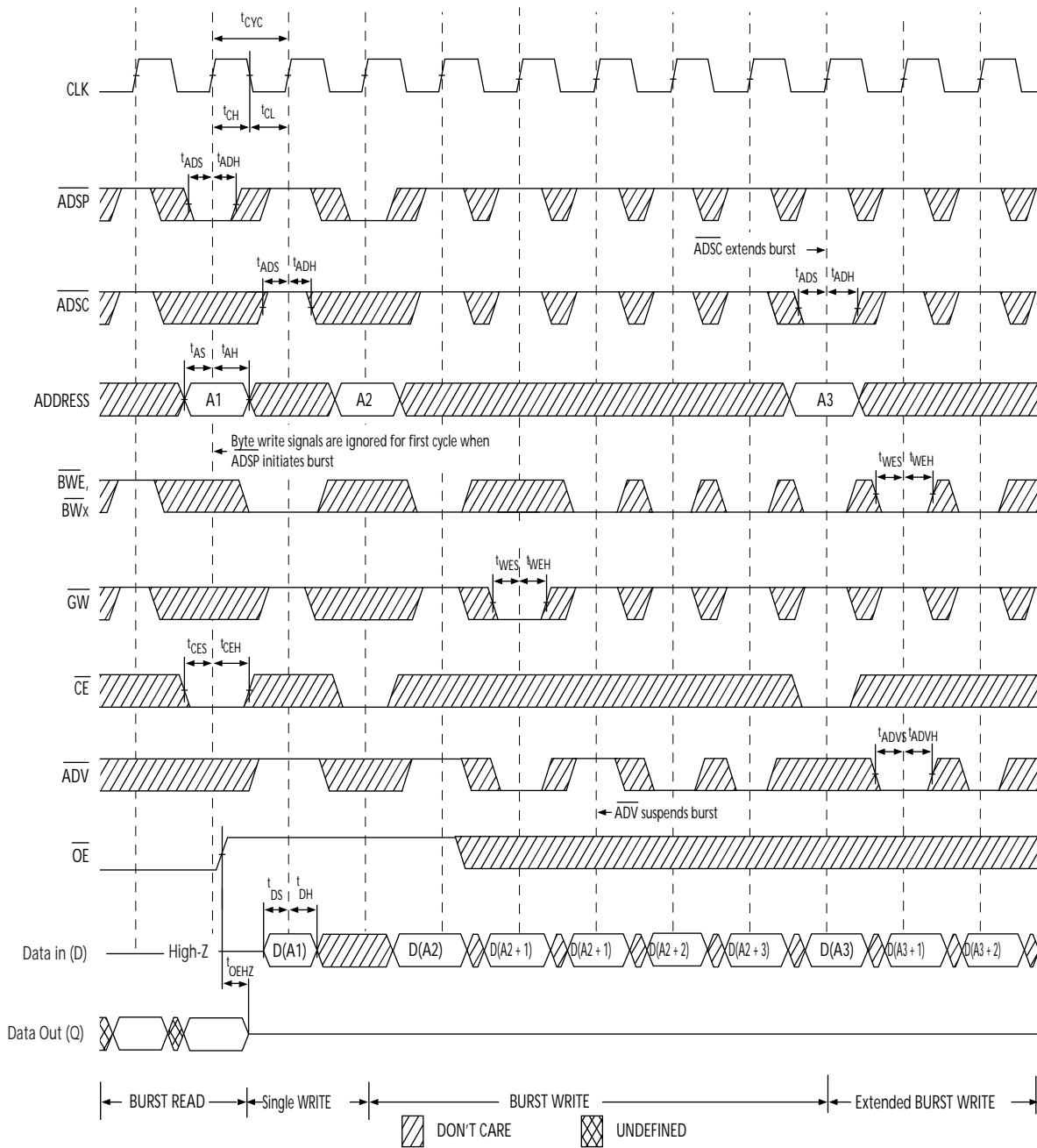
Notes
19. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
20. Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_X$ LOW.

Switching Waveforms *(continued)*

Figure 5. Read/Write Cycle Timing [21, 22, 23]

| DON'T CARE |
| UNDEFINED |
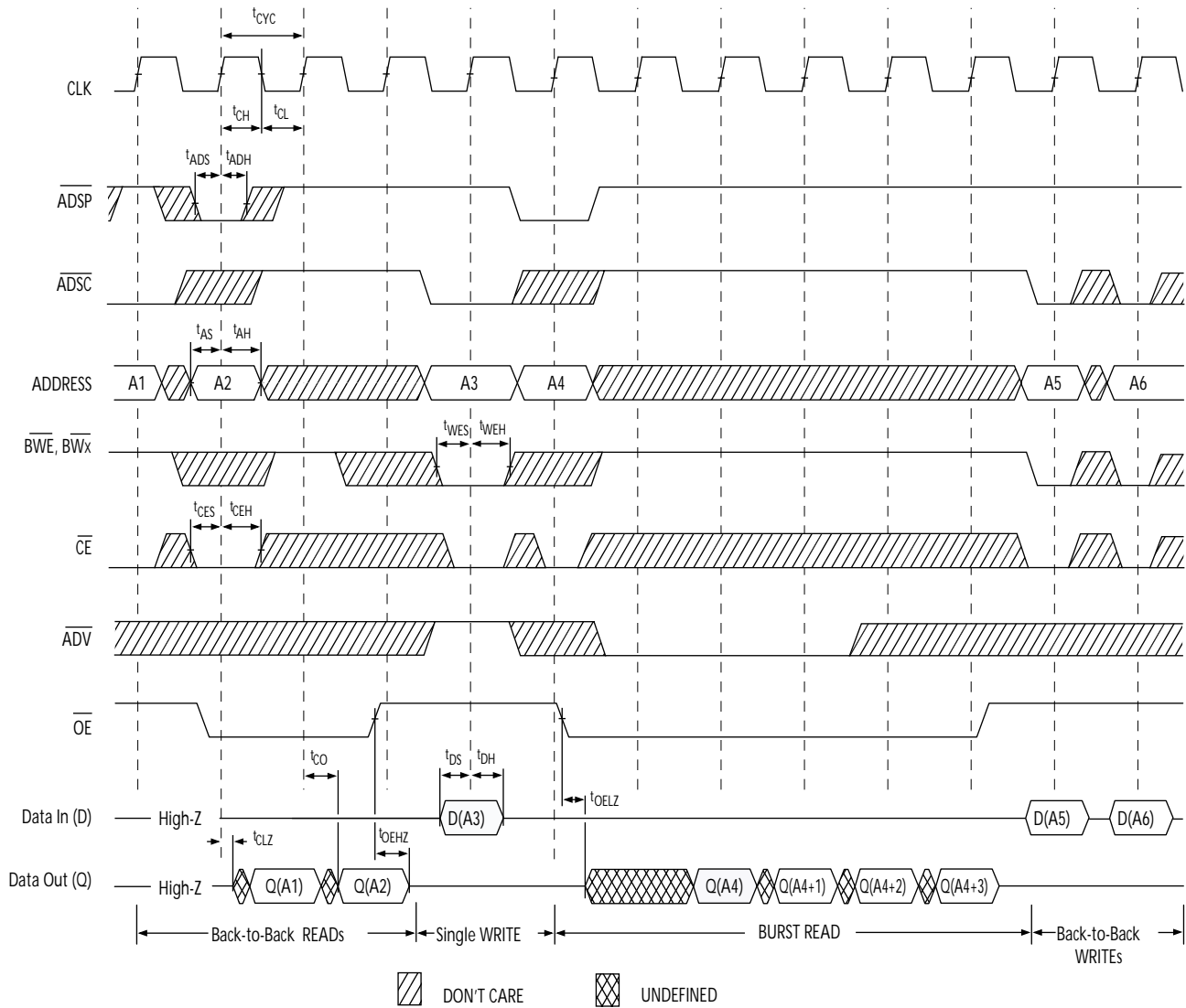
Notes
21. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE_1}$ is LOW, CE_2 is HIGH and $\overline{CE_3}$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE_1}$ is HIGH or CE_2 is LOW or $\overline{CE_3}$ is HIGH.
22. The data bus (Q) remains in high Z following a Write cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
23. GW is HIGH.

Switching Waveforms *(continued)*

Figure 6. ZZ Mode Timing [24, 25]

DON'T CARE
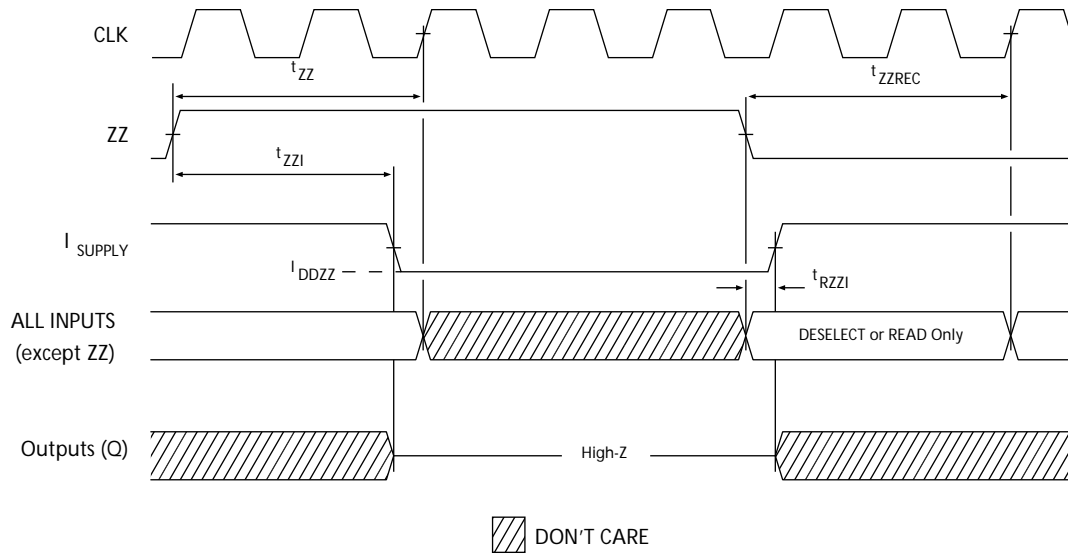
Notes
24. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
25. DQs are in high Z when exiting ZZ sleep mode.

Ordering Information

Table 1 lists the ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

Table 1. Ordering Information

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
250	CY7C1444KV33-250AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1445KV33-250AXC			

Ordering Code Definitions

CY 7 C 14XX K V33 - 250 A X C

Temperature range:
C = Commercial

Pb-free

Package Type:
A = 100-pin TQFP

Speed Grade: 250 MHz

V33 = 3.3 V

Process Technology: K = 65 nm

1444 = DCD, 1Mb × 36 (36Mb); 1445 = DCD, 2Mb × 18(36Mb)

Technology Code: C = CMOS

Marketing Code: 7 = SRAM

Company ID: CY = Cypress
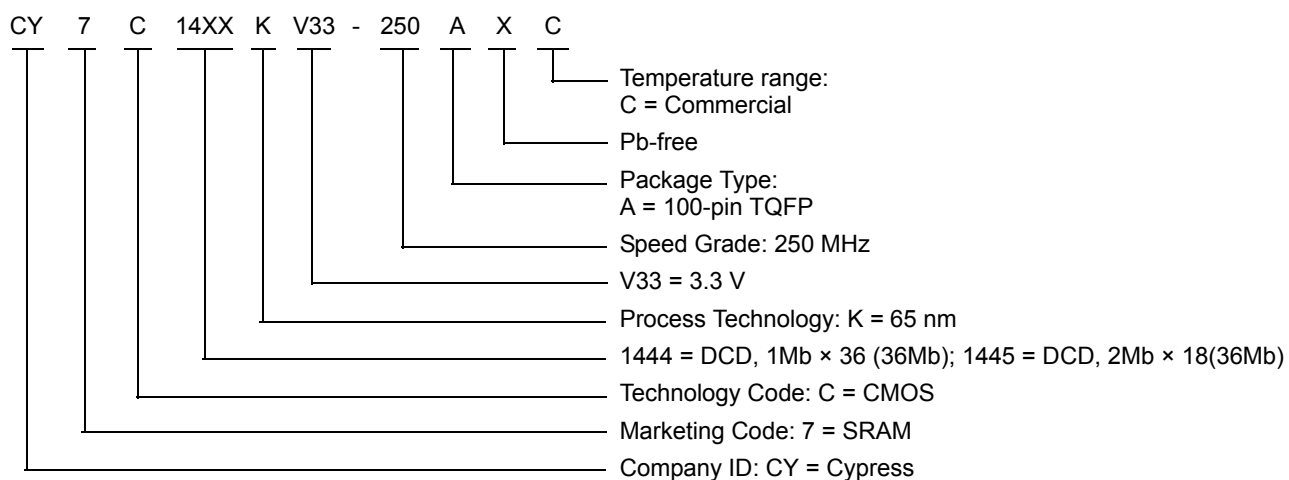
Package Diagram

Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050

NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050 *E
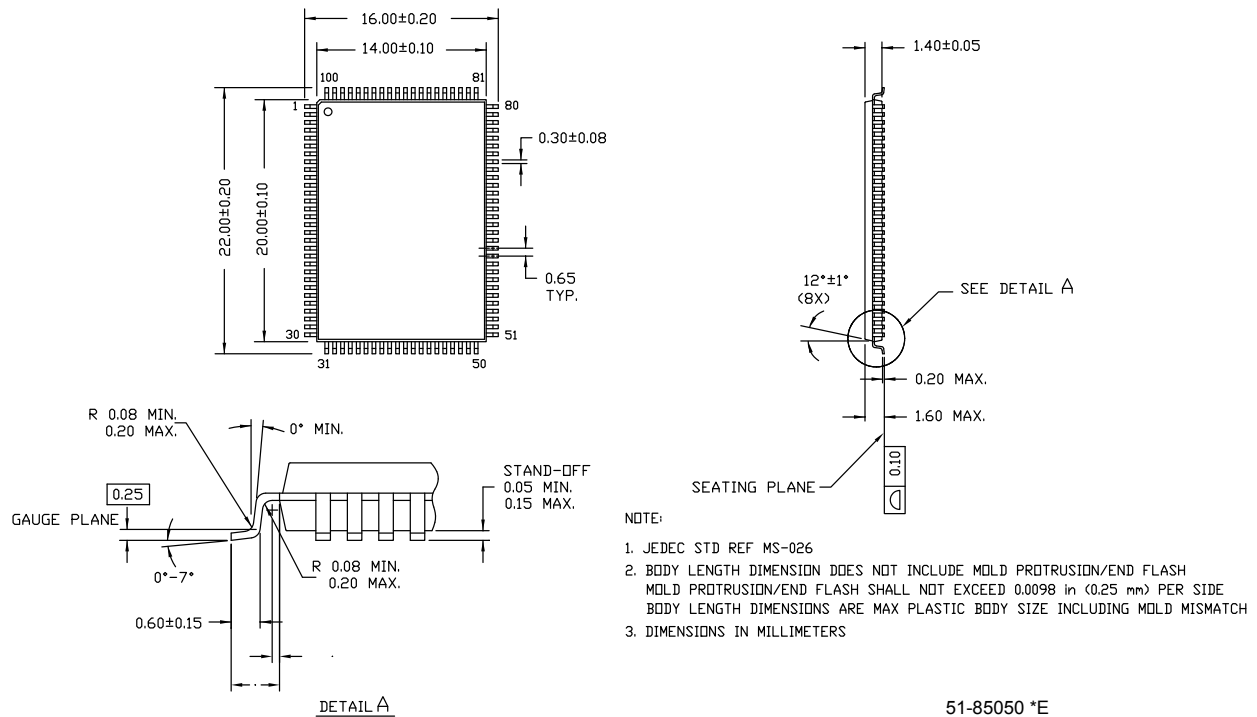
Acronyms

Table 2. Acronyms Used in this Document

Acronym	Description
$\overline{CE}$	Chip Enable
I/O	Input/Output
NoBL	No Bus Latency
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Table 3. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
ns	nanosecond
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1444KV33/CY7C1445KV33, 36-Mbit (1M × 36/2M × 18) Pipelined DCD Sync SRAM Document Number: 001-66678				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
*E	4680529	04/09/2015	PRIT	Changed status from Preliminary to Final.
*F	4757974	05/07/2015	DEVM	Updated Functional Overview: Updated ZZ Mode Electrical Characteristics: Changed maximum value of I_{DDZZ} parameter from 89 mA to 75 mA.
*G	5337537	07/05/2016	PRIT	Updated Neutron Soft Error Immunity: Updated values in "Typ" and "Max" columns corresponding to LSBU parameter. Updated to new template.

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