True 18-Bit, Voltage Output DAC ±0.5 LSB INL, ±0.5 LSB DNL

Data Sheet

AD5781

FEATURES

Single 18-bit DAC, ±0.5 LSB INL
7.5 nV/√Hz noise spectral density
0.05 LSB long-term linearity stability
<0.05 ppm/°C temperature drift
1 µs settling time
1.4 nV-sec glitch impulse
Operating temperature range: −40°C to +125°C
20-lead TSSOP package
Wide power supply range of up to ±16.5 V
35 MHz Schmitt triggered digital interface
1.8 V compatible digital interface

APPLICATIONS

Medical instrumentation
Test and measurement
Industrial control
Scientific and aerospace instrumentation
Data acquisition systems
Digital gain and offset adjustment
Power supply control

FUNCTIONAL BLOCK DIAGRAM

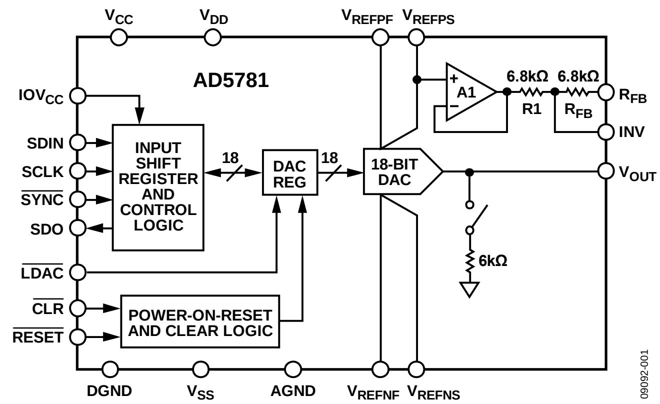

Figure 1.

Table 1. Complementary Devices

Part No.	Description
AD8675	Ultraprecision, 36 V, 2.8 nV/√Hz rail-to-rail output op amp
AD8676	Ultraprecision, 36 V, 2.8 nV/√Hz dual rail-to-rail output op amp
ADA4898-1	High voltage, low noise, low distortion, unity gain stable, high speed op amp

Table 2. Related Devices

Part No.	Description
AD5791	20-bit, 1 ppm accurate DAC
AD5541A/AD5542A	16-bit, 1 LSB accurate 5 V DAC

GENERAL DESCRIPTION

The AD5781[1] is a single 18-bit, unbuffered voltage output DAC that operates from a bipolar supply of up to 33 V. The AD5781 accepts a positive reference input range of 5 V to V_{DD} – 2.5 V and a negative reference input range of V_{SS} + 2.5 V to 0 V. The AD5781 offers a relative accuracy specification of ±0.5 LSB maximum, and operation is guaranteed monotonic with a ±0.5 LSB DNL maximum specification.

The part uses a versatile 3-wire serial interface that operates at clock rates of up to 35 MHz and is compatible with standard SPI, QSPI™, MICROWIRE™, and DSP interface standards. The part incorporates a power-on reset circuit that ensures that the DAC output powers up to 0 V and in a known output impedance state and remains in this state until a valid write to the device takes place. The part provides an output clamp feature that places the output in a defined load state.

PRODUCT HIGHLIGHTS

1. True 18-Bit Accuracy.
2. Wide Power Supply Range of Up to ±16.5 V.
3. −40°C to +125°C Operating Temperature Range.
4. Low 7.5 nV/√Hz Noise.
5. Low 0.05 ppm/°C Temperature Drift.

[1] Protected by U.S. Patent No 7884747, and other patents are pending.

Rev. D Document Feedback

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AD5781* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD5781 Evaluation Board

DOCUMENTATION

Data Sheet

- AD5781-DSCC: Military Data Sheet
- AD5781-EP: Enhanced Product Data Sheet
- AD5781: True 18-Bit, Voltage Output DAC ±0.5 LSB INL, ±0.5 LSB DNL Data Sheet

User Guides

- AD5781/AD5791 Quick Start Guide
- UG-184: Evaluation Board for a 18-Bit Serial Input, Voltage Output DAC

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD5780 - Microcontroller No-OS Driver
- AD5781 - No-OS Driver for Microchip Microcontroller Platforms
- AD5781 - No-OS Driver for Renesas Microcontroller Platforms
- AD5781 Pmod Xilinx FPGA Reference Design
- AD5781 FMC-SDP Interposer & Evaluation Board / Xilinx KC705 Reference Design
- BeMicro FPGA Project for AD5781 with Nios driver

REFERENCE DESIGNS

- CN0177

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Digital to Analog Converters ICs Solutions Bulletin

DESIGN RESOURCES

- AD5781 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD5781 EngineerZone Discussions.

SAMPLE AND BUY

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7/10—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = +12.5 V to +16.5 V, V_{SS} = −16.5 V to −12.5 V, V_{REFP} = +10 V, V_{REFN} = −10 V, V_{CC} = +2.7 V to +5.5 V, IOV_{CC} = +1.71 V to +5.5 V, R_L = unloaded, C_L = unloaded, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	A, B Version[1] Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE[2]					
Resolution	18			Bits	
Integral Nonlinearity Error (Relative Accuracy)	−0.5	±0.25	+0.5	LSB	B version, V_{REFP} = +10 V, V_{REFN} = −10 V
	−0.5	±0.25	+0.5	LSB	B version, V_{REFP} = +10 V, V_{REFN} = 0 V[3]
	−1	±0.5	+1	LSB	B version, V_{REFP} = +5 V, V_{REFN} = 0 V[3]
	−4	±2	+4	LSB	A version[4]
Differential Nonlinearity Error	−0.5	±0.25	+0.5	LSB	V_{REFP} = +10 V, V_{REFN} = −10 V
	−0.5	±0.25	+0.5	LSB	V_{REFP} = +10 V, V_{REFN} = 0 V[3]
	−1	±0.5	+1	LSB	V_{REFP} = +5 V, V_{REFN} = 0 V[3]
Linearity Error Long-Term Stability[5]		0.04		LSB	After 500 hours at T_A = 125°C
		0.05		LSB	After 1000 hours at T_A = 125°C
		0.03		LSB	After 1000 hours t T_A = 100°C
Full-Scale Error	−1.75	±0.25	+1.75	LSB	V_{REFP} = +10 V, V_{REFN} = −10 V[3]
	−2.75	±0.062	+2.75	LSB	V_{REFP} = +10 V, V_{REFN} = 0 V[3]
	−5.25	±0.2	+5.25	LSB	V_{REFP} = +5 V, V_{REFN} = 0 V[3]
	−1	±0.25	+1	LSB	V_{REFP} = +10 V, V_{REFN} = −10 V[3], T_A = 0°C to 105°C
	−1	±0.062	+1	LSB	V_{REFP} = 10 V, V_{REFN} = 0 V[3], T_A = 0°C to 105°C
	−1.5	±0.2	+1.5	LSB	V_{REFP} = 5 V, V_{REFN} = 0 V[3], T_A = 0°C to 105°C
Full-Scale Error Temperature Coefficient[3]		±0.02		ppm FSR/°C	
Zero-Scale Error	−1.75	±0.025	+1.75	LSB	V_{REFP} = +10 V, V_{REFN} = −10 V[3]
	−2.5	±0.38	+2.5	LSB	V_{REFP} = +10 V, V_{REFN} = 0 V[3]
	−5.25	±0.19	+5.25	LSB	V_{REFP} = +5 V, V_{REFN} = 0 V[3]
	−1	±0.025	+1	LSB	V_{REFP} = +10 V, V_{REFN} = −10 V[3], T_A = 0°C to 105°C
	−1	±0.38	+1	LSB	V_{REFP} = 10 V, V_{REFN} = 0 V[3], T_A = 0°C to 105°C
	−1.5	±0.19	+1.5	LSB	V_{REFP} = 5 V, V_{REFN} = 0 V[3], T_A = 0°C to 105°C
Zero-Scale Error Temperature Coefficient[3]		±0.04		ppm FSR/°C	
Gain Error	−6	±0.3	+6	ppm FSR	V_{REFP} = +10 V, V_{REFN} = −10 V[3]
	−10	±0.4	+10	ppm FSR	V_{REFP} = +10 V, V_{REFN} = 0 V[3]
	−20	±0.4	+20	ppm FSR	V_{REFP} = +5 V, V_{REFN} = 0 V[3]
Gain Error Temperature Coefficient[3]		±0.04		ppm FSR/°C	
R1, R_{FB} Matching		0.01		%	
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	V_{REFN}		V_{REFP}	V	
Output Slew Rate		50		V/µs	Unbuffered output, 10 MΩ‖20 pF load
Output Voltage Settling Time		1		µs	10 V step to 0.02%, using AD845 buffer in unity-gain mode
		1		µs	125 code step to ±1 LSB[6]
Output Noise Spectral Density		7.5		nV/√Hz	at 1 kHz, DAC code = midscale
		7.5		nV/√Hz	at 10 kHz, DAC code = midscale
		7.5		nV/√Hz	at 100 kHz, DAC code = midscale
Output Voltage Noise		1.1		µV p-p	DAC code = midscale, 0.1 Hz to 10 Hz bandwidth[7]

Parameter	A, B Version[1] Min	Typ	Max	Unit	Test Conditions/Comments
Midscale Glitch Impulse		3.1		nV-sec	V_{REFP} = +10 V, V_{REFN} = −10 V
		1.7		nV-sec	V_{REFP} = +10 V, V_{REFN} = 0 V
		1.4		nV-sec	V_{REFP} = +5 V, V_{REFN} = 0 V
MSB Segment Glitch Impulse[6]		9.1		nV-sec	V_{REFP} = +10 V, V_{REFN} = −10 V, see Figure 42
		3.6		nV-sec	V_{REFP} = 10 V, V_{REFN} = 0 V, see Figure 43
		1.9		nV-sec	V_{REFP} = 5 V, V_{REFN} = 0 V, see Figure 44
Output Enabled Glitch Impulse		45		nV-sec	On removal of output ground clamp
Digital Feedthrough		0.4		nV-sec	
DC Output Impedance (Normal Mode)		3.4		kΩ	
DC Output Impedance (Output Clamped to Ground)		6		kΩ	
Spurious Free Dynamic Range		100		dB	1 kHz tone, 10 kHz sample rate
Total Harmonic Distortion		97		dB	1 kHz tone, 10 kHz sample rate
REFERENCE INPUTS[3]					
V_{REFP} Input Range	5		V_{DD} − 2.5 V	V	
V_{REFN} Input Range	V_{SS} + 2.5 V		0		
DC Input Impedance	5	6.6		kΩ	V_{REFP}, V_{REFN}, code dependent, typical at midscale code
Input Capacitance		15		pF	V_{REFP}, V_{REFN}
LOGIC INPUTS[3]					
Input Current[8]	−1		+1	µA	
Input Low Voltage, V_{IL}			0.3 × IOV_{CC}	V	IOV_{CC} = 1.71 V to 5.5 V
Input High Voltage, V_{IH}	0.7 × IOV_{CC}			V	IOV_{CC} = 1.71 V to 5.5 V
Pin Capacitance		5		pF	
LOGIC OUTPUT (SDO)[3]					
Output Low Voltage, V_{OL}			0.4	V	IOV_{CC} = 1.71 V to 5.5 V, sinking 1 mA
Output High Voltage, V_{OH}	IOV_{CC} − 0.5 V				IOV_{CC} = 1.71 V to 5.5 V, sourcing 1 mA
High Impedance Leakage Current			±1	µA	
High Impedance Output Capacitance		3		pF	
POWER REQUIREMENTS					All digital inputs at DGND or IOV_{CC}
V_{DD}	7.5		V_{SS} + 33	V	
V_{SS}	V_{DD} − 33		−2.5	V	
V_{CC}	2.7		5.5	V	
IOV_{CC}	1.71		5.5	V	$IOV_{CC} \leq V_{CC}$
I_{DD}		4.2	5.2	mA	
I_{SS}		4	4.9	mA	
I_{CC}		600	900	µA	
IOI_{CC}		52	140	µA	SDO disabled
DC Power Supply Rejection Ratio[3, 9]		±0.6		µV/V	V_{DD} ± 10%, V_{SS} = 15 V
		±0.6		µV/V	V_{SS} ± 10%, V_{DD} = 15 V
AC Power Supply Rejection Ratio[3]		95		dB	V_{DD} ± 200 mV, 50 Hz/60 Hz, V_{SS} = −15 V
		95		dB	V_{SS} ± 200 mV, 50 Hz/60 Hz, V_{DD} = 15 V

[1] Temperature range: −40°C to +125°C, typical conditions: T_A = 25°C, V_{DD} = +15 V, V_{SS} = −15 V, V_{REFP} = +10 V, V_{REFN} = −10 V.
[2] Performance characterized with AD8676BRZ voltage reference buffers and AD8675ARZ output buffer.
[3] Linearity error refers to both INL error and DNL error; either parameter can be expected to drift by the amount specified after the length of time specified.
[4] Valid for all voltage reference spans.
[5] Guaranteed by design and characterization, not production tested.
[6] The AD5781 is configured in the bias compensation mode with a low-pass RC filter on the output. R = 300 Ω, C = 143 pF (total capacitance seen by the output buffer, lead capacitance, and so forth).
[7] Includes noise contribution from AD8676BRZ voltage reference buffers.
[8] Current flowing in an individual logic pin.
[9] Includes PSRR of AD8676BRZ voltage reference buffers.

TIMING CHARACTERISTICS

V_{CC} = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter	Limit[1] IOV$_{CC}$ = 1.71 V to 3.3 V	IOV$_{CC}$ = 3.3 V to 5.5 V	Unit	Test Conditions/Comments
t_1[2]	40	28	ns min	SCLK cycle time
	92	60	ns min	SCLK cycle time (readback mode)
t_2	15	10	ns min	SCLK high time
t_3	9	5	ns min	SCLK low time
t_4	5	5	ns min	$\overline{\text{SYNC}}$ to SCLK falling edge setup time
t_5	2	2	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge hold time
t_6	48	40	ns min	Minimum $\overline{\text{SYNC}}$ high time
t_7	8	6	ns min	$\overline{\text{SYNC}}$ rising edge to next SCLK falling edge ignore
t_8	9	7	ns min	Data setup time
t_9	12	7	ns min	Data hold time
t_{10}	13	10	ns min	$\overline{\text{LDAC}}$ falling edge to $\overline{\text{SYNC}}$ falling edge
t_{11}	20	16	ns min	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge
t_{12}	14	11	ns min	$\overline{\text{LDAC}}$ pulse width low
t_{13}	130	130	ns typ	$\overline{\text{LDAC}}$ falling edge to output response time
t_{14}	130	130	ns typ	$\overline{\text{SYNC}}$ rising edge to output response time ($\overline{\text{LDAC}}$ tied low)
t_{15}	50	50	ns min	$\overline{\text{CLR}}$ pulse width low
t_{16}	140	140	ns typ	$\overline{\text{CLR}}$ pulse activation time
t_{17}	0	0	ns min	$\overline{\text{SYNC}}$ falling edge to first SCLK rising edge
t_{18}	65	60	ns max	$\overline{\text{SYNC}}$ rising edge to SDO tristate (C_L = 50 pF)
t_{19}	62	45	ns max	SCLK rising edge to SDO valid (C_L = 50 pF)
t_{20}	0	0	ns min	$\overline{\text{SYNC}}$ rising edge to SCLK rising edge ignore
t_{21}	35	35	ns typ	$\overline{\text{RESET}}$ pulse width low
t_{22}	150	150	ns typ	$\overline{\text{RESET}}$ pulse activation time

[1] All input signals are specified with t_R = t_F = 1 ns/V (10% to 90% of IOV$_{CC}$) and timed from a voltage level of (V_{IL} + V_{IH})/2.
[2] Maximum SCLK frequency is 35 MHz for write mode and 16 MHz for readback mode.

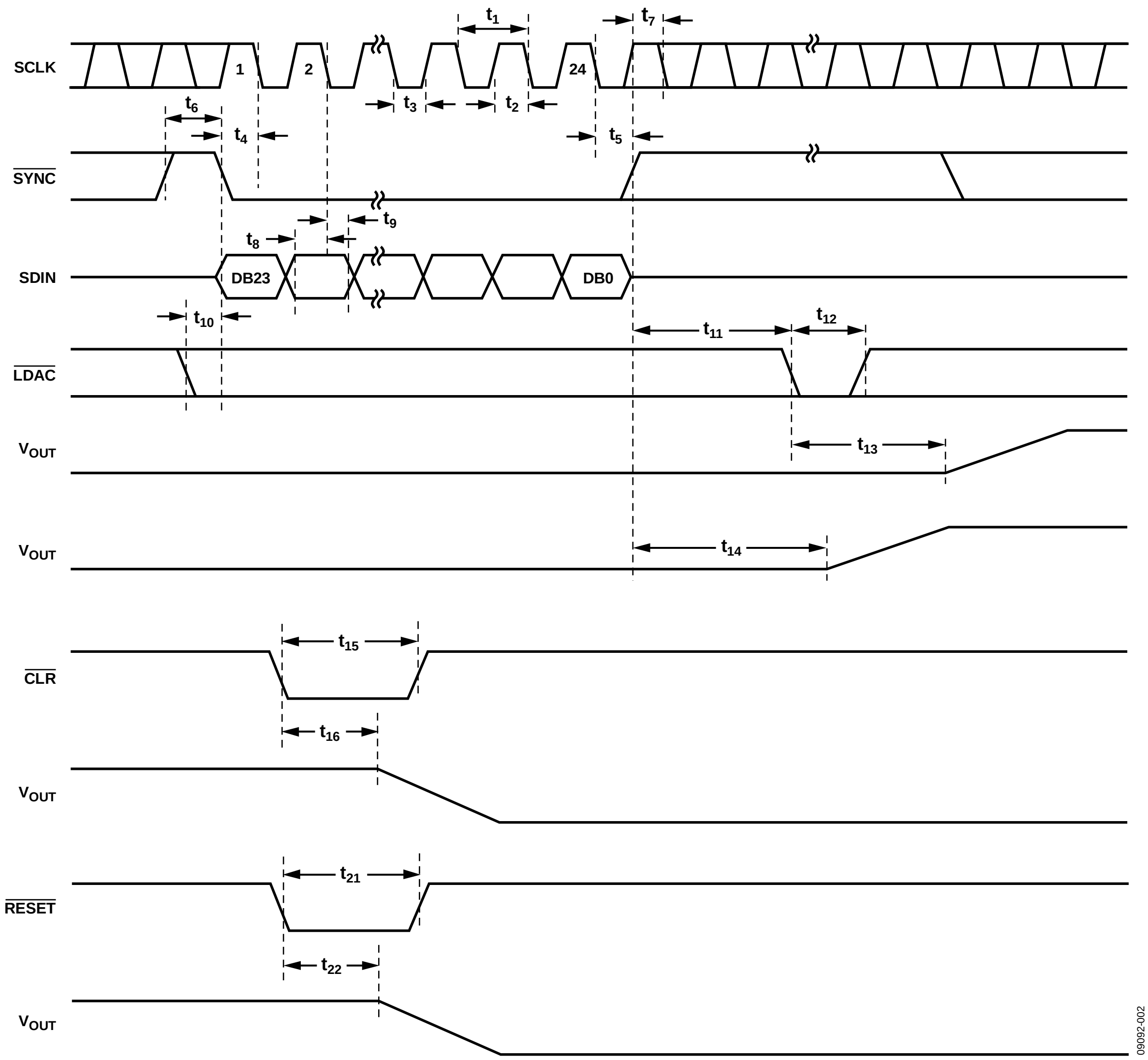


Figure 2. Write Mode Timing Diagram

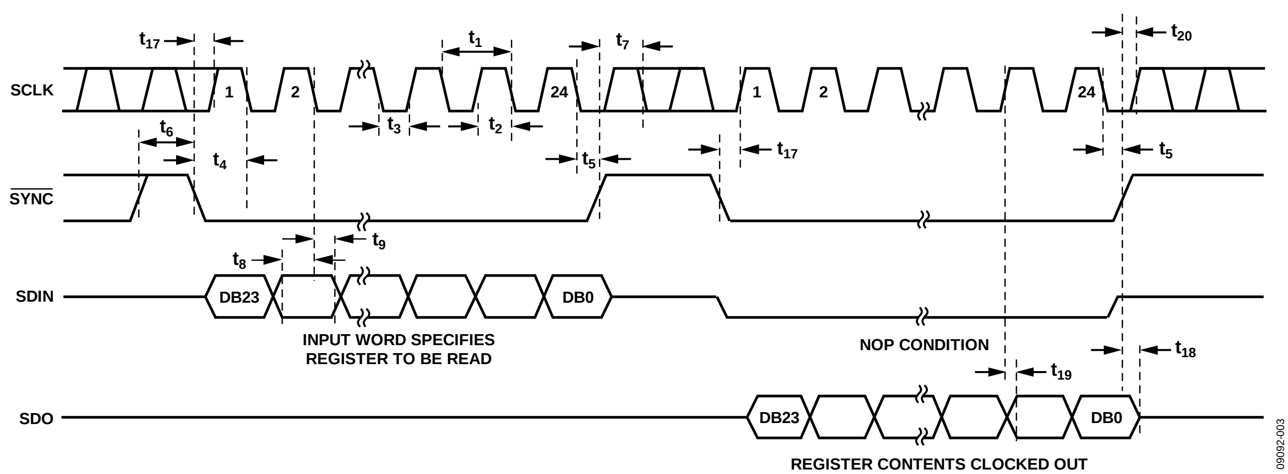


Figure 3. Readback Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

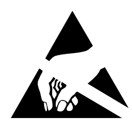
Table 5.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +34 V
V_{SS} to AGND	−34 V to +0.3 V
V_{DD} to V_{SS}	−0.3 V to +34 V
V_{CC} to DGND	−0.3 V to +7 V
IOV_{CC} to DGND	−0.3 V to V_{CC} + 3 V or +7 V (whichever is less)
Digital Inputs to DGND	−0.3 V to IOV_{CC} + 0.3 V or +7 V (whichever is less)
V_{OUT} to AGND	−0.3 V to V_{DD} + 0.3 V
V_{REFPF} to AGND	−0.3 V to V_{DD} + 0.3 V
V_{REFPS} to AGND	−0.3 V to V_{DD} + 0.3 V
V_{REFNF} to AGND	V_{SS} − 0.3 V to +0.3 V
V_{REFNS} to AGND	V_{SS} − 0.3 V to +0.3 V
DGND to AGND	−0.3 V to +0.3 V
Operating Temperature Range, T_A	
Industrial	−40°C to + 125°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature, T_J max	150°C
Power Dissipation	(T_J max − T_A)/θ_{JA}
TSSOP Package	
θ_{JA} Thermal Impedance	143°C/W
θ_{JC} Thermal Impedance	45°C/W
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020
ESD (Human Body Model)	1.5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance integrated circuit with an ESD rating of 1.5 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

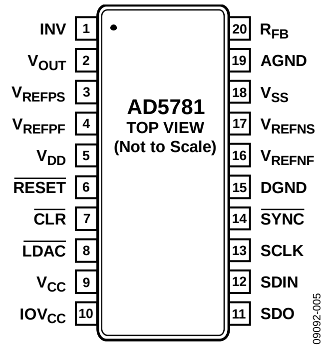


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INV	Connection to Inverting Input of External Amplifier. See the AD5781 Features section for further details.
2	V_{OUT}	Analog Output Voltage.
3	V_{REFPS}	Positive Reference Sense Voltage Input. A voltage range of 5 V to V_{DD} − 2.5 V can be connected. A unity gain amplifier must be connected at this pin, in conjunction with the V_{REFPF} pin. See the AD5781 Features section for further details.
4	V_{REFPF}	Positive Reference Force Voltage Input. A voltage range of 5 V to V_{DD} − 2.5 V can be connected. A unity gain amplifier must be connected at these pin, in conjunction with the V_{REFPS} pin. See AD5781 Features section for further details.
5	V_{DD}	Positive Analog Supply Connection. A voltage range of 7.5 V to 16.5 V can be connected. V_{DD} should be decoupled to AGND.
6	$\overline{\text{RESET}}$	Active Low Reset Logic Input Pin. Asserting this pin returns the AD5781 to its power-on status.
7	$\overline{\text{CLR}}$	Active Low Clear Logic Input Pin. Asserting this pin sets the DAC register to a user defined value (see Table 13) and updates the DAC output. The output value depends on the DAC register coding that is being used, either binary or twos complement.
8	$\overline{\text{LDAC}}$	Active Low Load DAC Logic Input Pin. This is used to update the DAC register and, consequently, the analog output. When tied permanently low, the output is updated on the rising edge of $\overline{\text{SYNC}}$. If $\overline{\text{LDAC}}$ is held high during the write cycle, the input register is updated, but the output update is held off until the falling edge of $\overline{\text{LDAC}}$. The $\overline{\text{LDAC}}$ pin should not be left unconnected.
9	V_{CC}	Digital Supply Connection. A voltage in the range of 2.7 V to 5.5 V can be connected. V_{CC} should be decoupled to DGND.
10	IOV_{CC}	Digital Interface Supply Pin. Digital threshold levels are referenced to the voltage applied to this pin. A voltage range of 1.71 V to 5.5 V can be connected. IOV_{CC} should not be allowed to exceed V_{CC}.
11	SDO	Serial Data Output Pin. Data is clocked out on the rising edge of the serial clock input.
12	SDIN	Serial Data Input Pin. This device has a 24-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
13	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at clock rates of up to 35 MHz.
14	$\overline{\text{SYNC}}$	Active Low Digital Interface Synchronization Input Pin. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ is low, it enables the input shift register, and data is then transferred in on the falling edges of the following clocks. The input shift register is updated on the rising edge of $\overline{\text{SYNC}}$.
15	DGND	Ground Reference Pin for Digital Circuitry.
16	V_{REFNF}	Negative Reference Force Voltage Input. A voltage range of V_{SS} + 2.5 V to 0 V can be connected. A unity gain amplifier must be connected at this pin, in conjunction with the V_{REFNS} pin. See the AD5781 Features section for further details.
17	V_{REFNS}	Negative Reference Sense Voltage Input. A voltage range of V_{SS} + 2.5 V to 0 V can be connected. A unity gain amplifier must be connected at these pin, in conjunction with the V_{REFNF} pin. See the AD5781 Features section for further details.
18	V_{SS}	Negative Analog Supply Connection. A voltage range of −16.5 V to −2.5 V can be connected. V_{SS} should be decoupled to AGND.
19	AGND	Ground Reference Pin for Analog Circuitry.
20	R_{FB}	Feedback Connection for External Amplifier. See the AD5781 Features section for further details.

TYPICAL PERFORMANCE CHARACTERISTICS

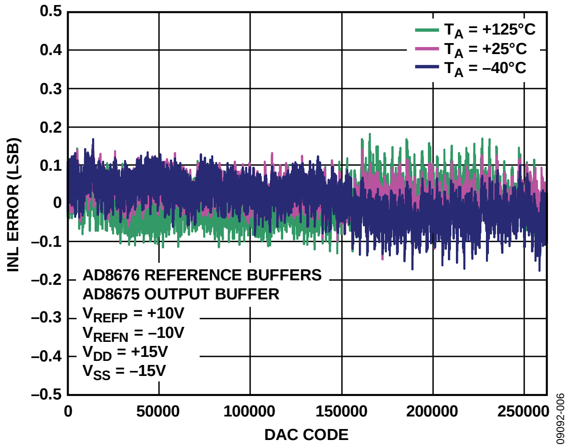


Figure 5. Integral Nonlinearity Error vs. DAC Code, ±10 V Span

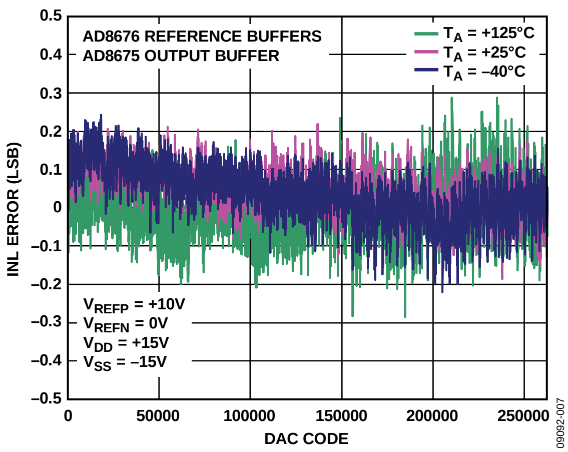


Figure 6. Integral Nonlinearity Error vs. DAC Code, +10 V Span

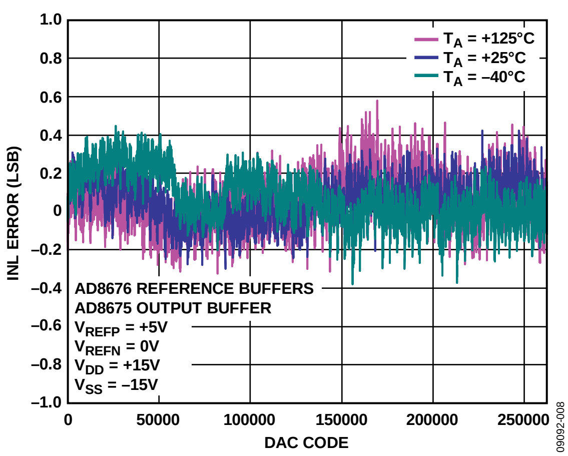


Figure 7. Integral Nonlinearity Error vs. DAC Code, +5 V Span

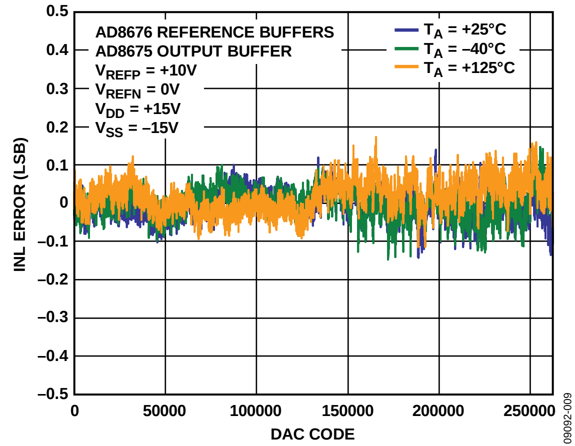


Figure 8. Integral Nonlinearity Error vs. DAC Code, ±10 V Span, X2 Gain Mode

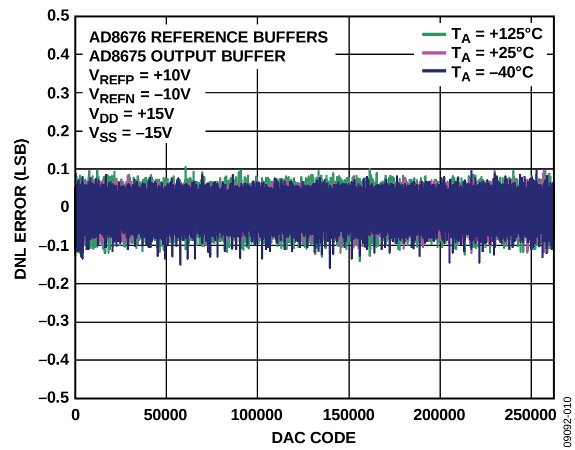


Figure 9. Differential Nonlinearity Error vs. DAC Code, ±10 V Span

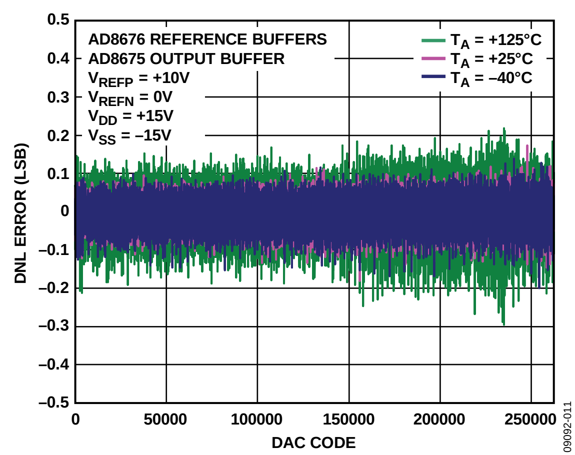


Figure 10. Differential Nonlinearity Error vs. DAC Code, +10 V Span

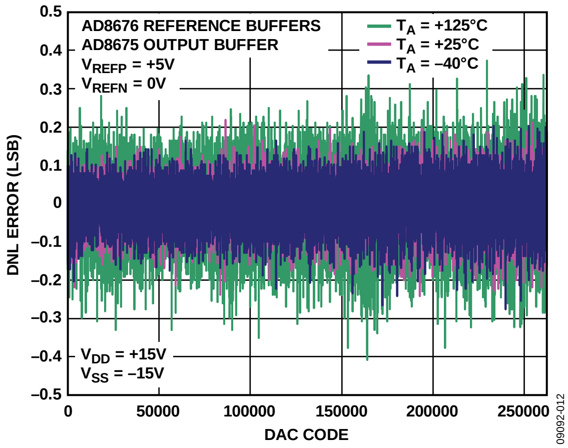


Figure 11. Differential Nonlinearity Error vs. DAC Code, +5 V Span

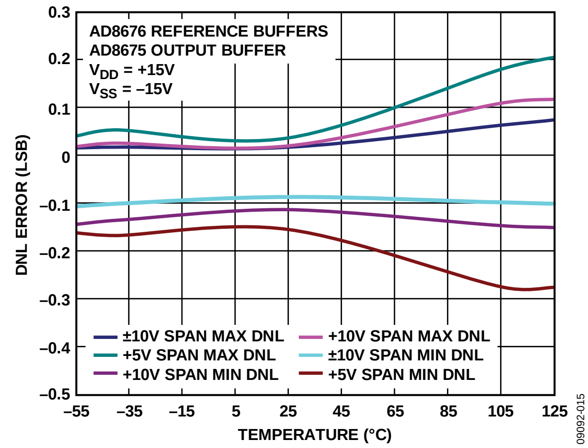


Figure 14. Differential Nonlinearity Error vs. Temperature

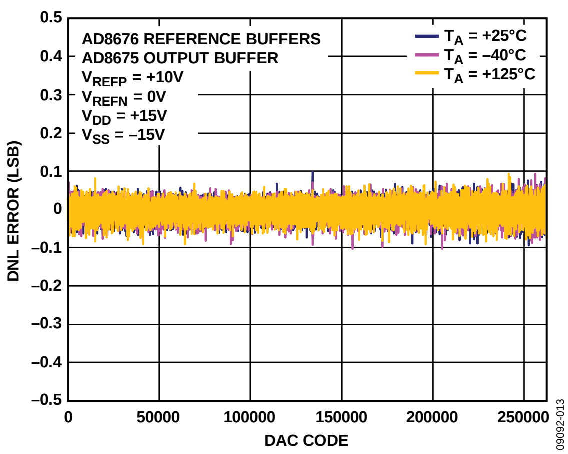


Figure 12. Differential Nonlinearity Error vs. DAC Code, ±10 V Span, X2 Gain Mode

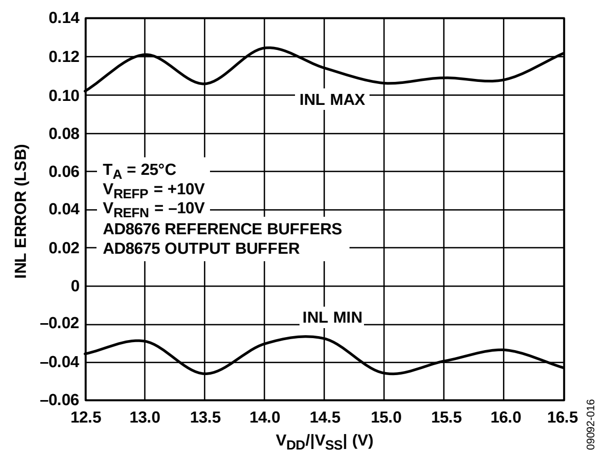


Figure 15. Integral Nonlinearity Error vs. Supply Voltage, ±10 V Span

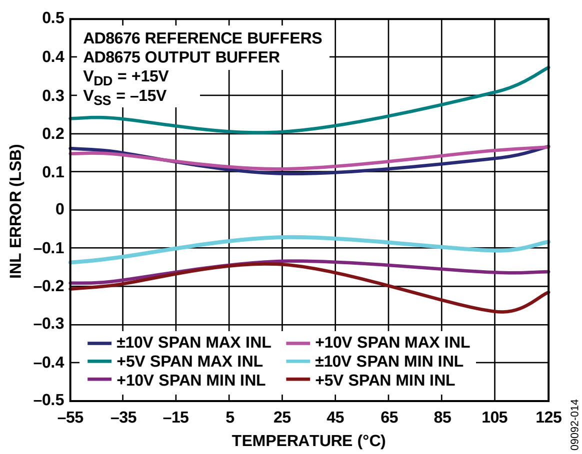


Figure 13. Integral Nonlinearity Error vs. Temperature

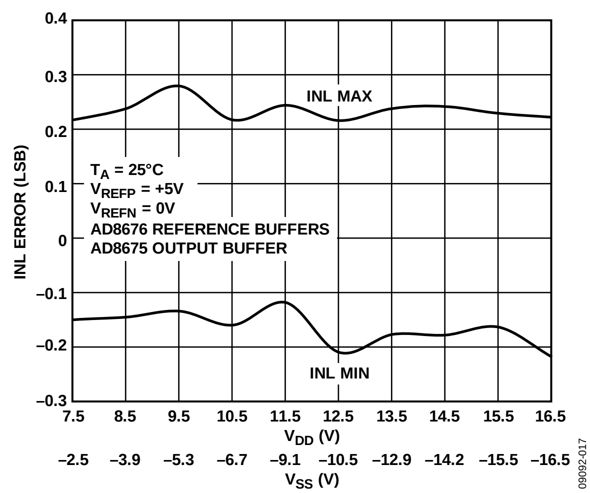


Figure 16. Integral Nonlinearity Error vs. Supply Voltage, +5 V Span

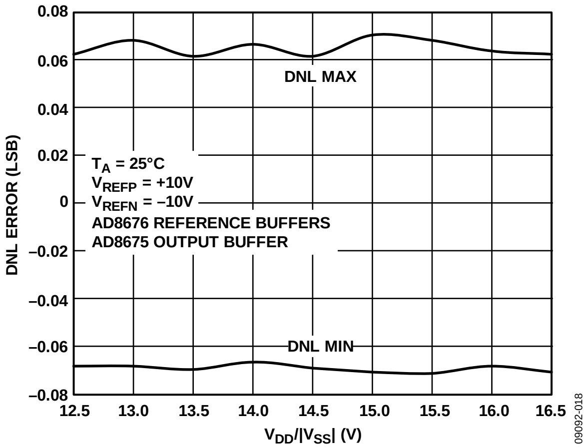


Figure 17. Differential Nonlinearity Error vs. Supply Voltage, ±10 V Span

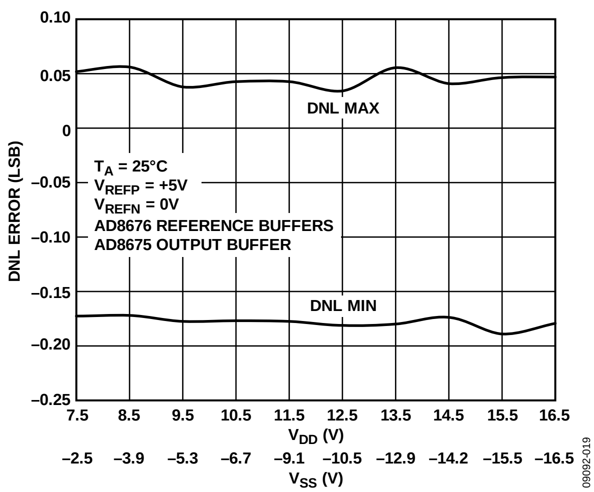


Figure 18. Differential Nonlinearity Error vs. Supply Voltage, +5 V Span

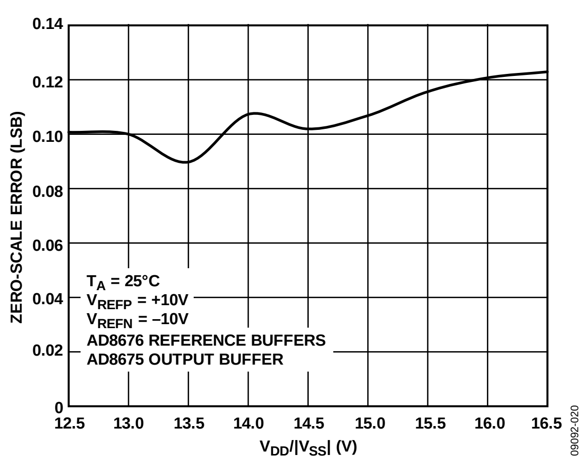


Figure 19. Zero-Scale Error vs. Supply Voltage, ±10 V Span

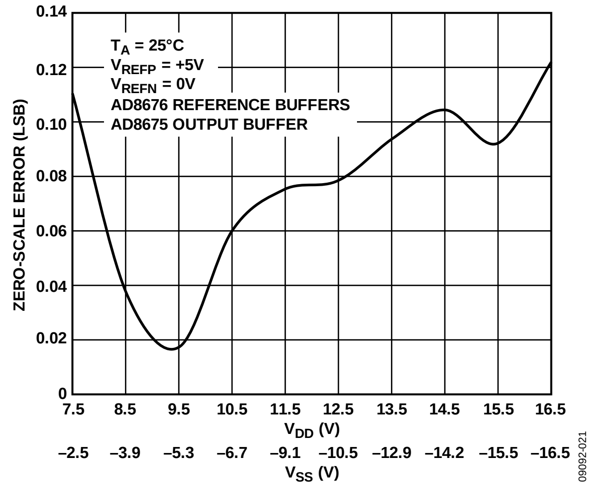


Figure 20. Zero-Scale Error vs. Supply Voltage, +5 V Span

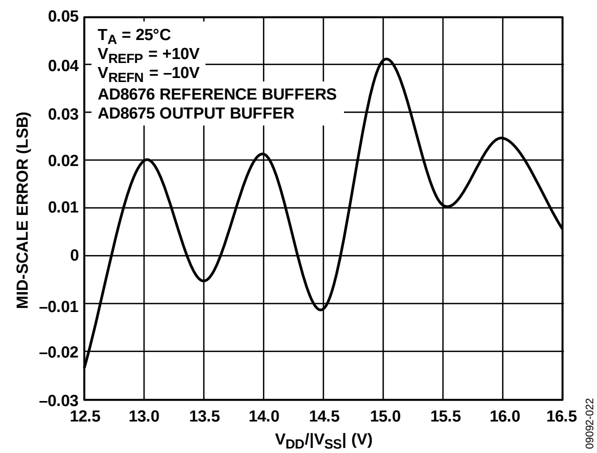


Figure 21. Midscale Error vs. Supply Voltage, ±10 V Span

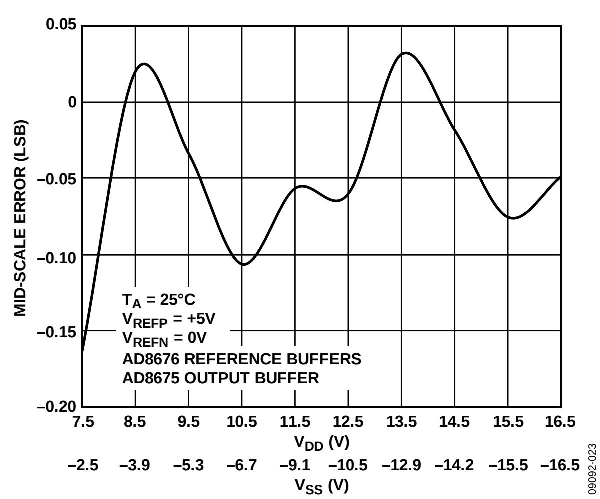


Figure 22. Midscale Error vs. Supply Voltage, +5 V Span

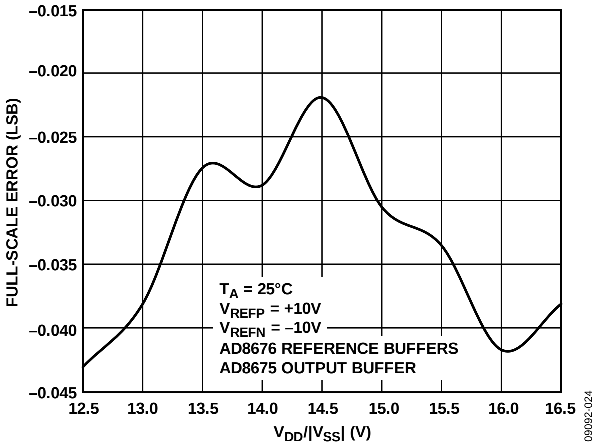


Figure 23. Full-Scale Error vs. Supply Voltage, ±10 V Span

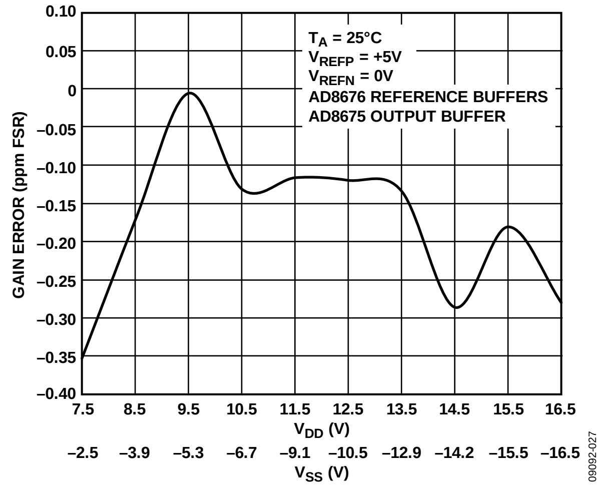


Figure 26. Gain Error vs. Supply Voltage, +5 V Span

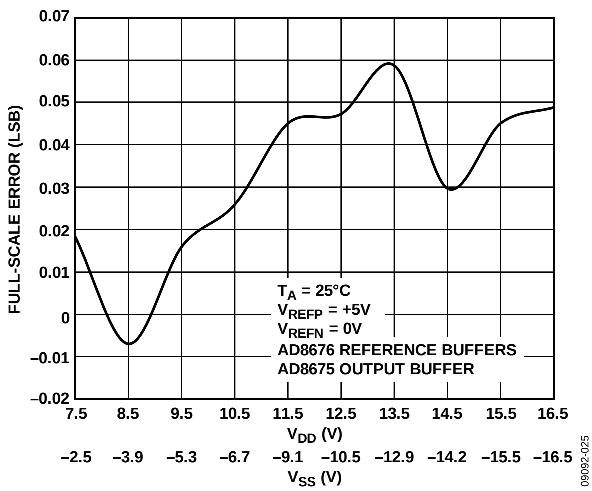


Figure 24. Full-Scale Error vs. Supply Voltage, +5 V Span

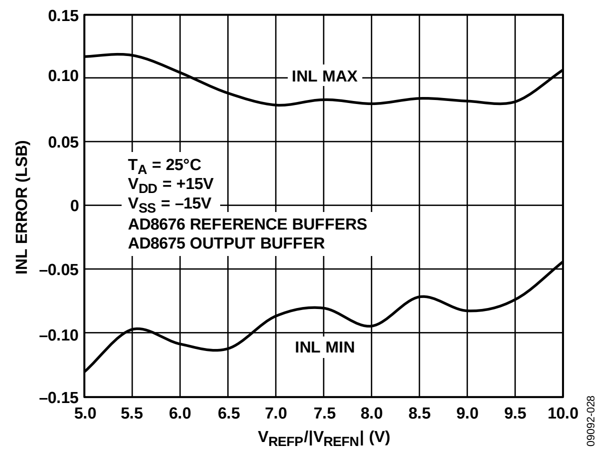


Figure 27. Integral Nonlinearity Error vs. Reference Voltage

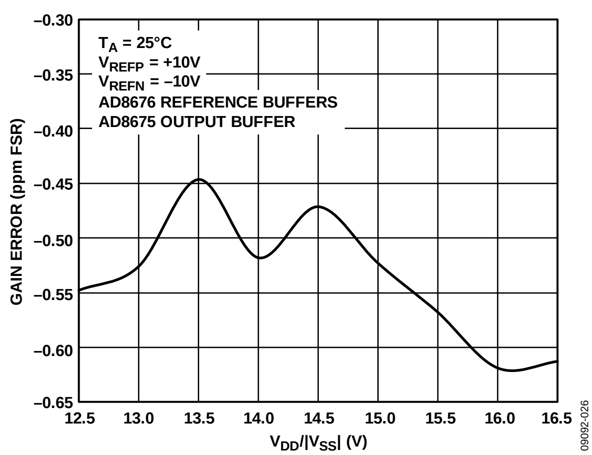


Figure 25. Gain Error vs. Supply Voltage, ±10 V Span

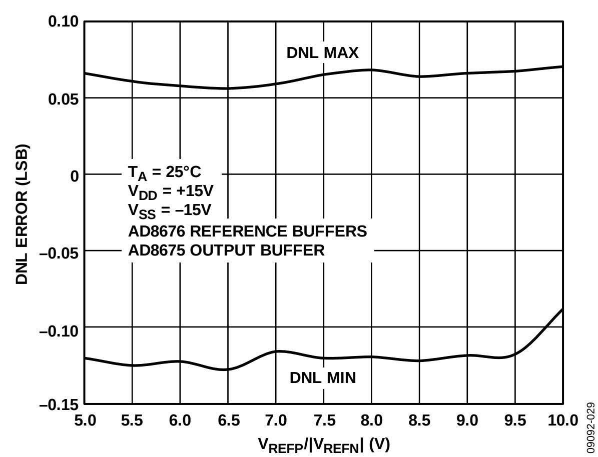


Figure 28. Differential Nonlinearity Error vs. Reference Voltage

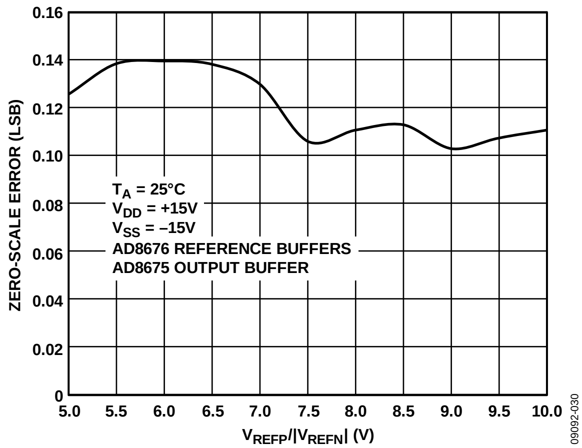


Figure 29. Zero-Scale Error vs. Reference Voltage

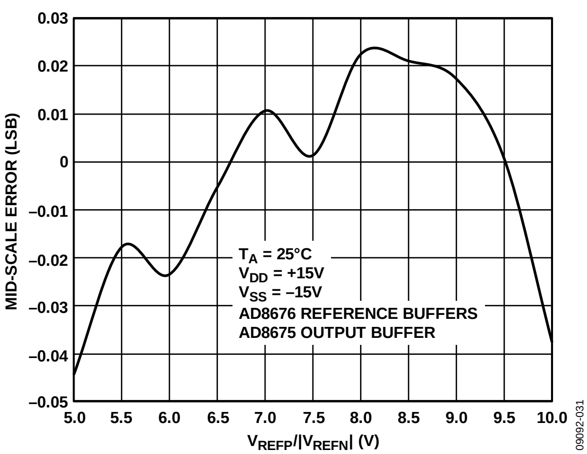


Figure 30. Midscale Error vs. Reference Voltage

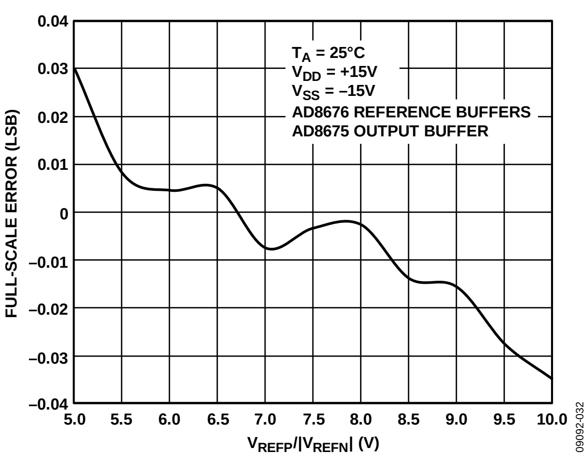


Figure 31. Full-Scale Error vs. Reference Voltage

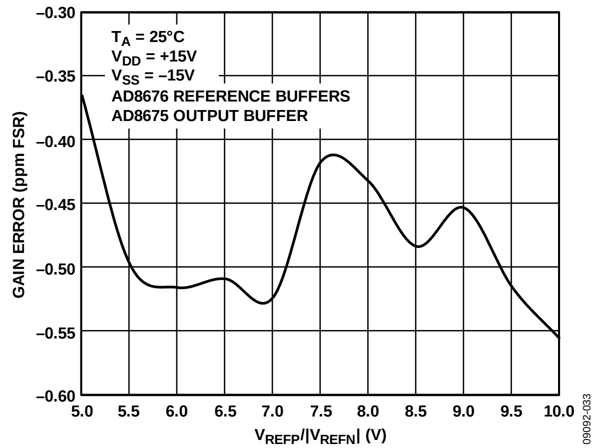


Figure 32. Gain Error vs. Reference Voltage

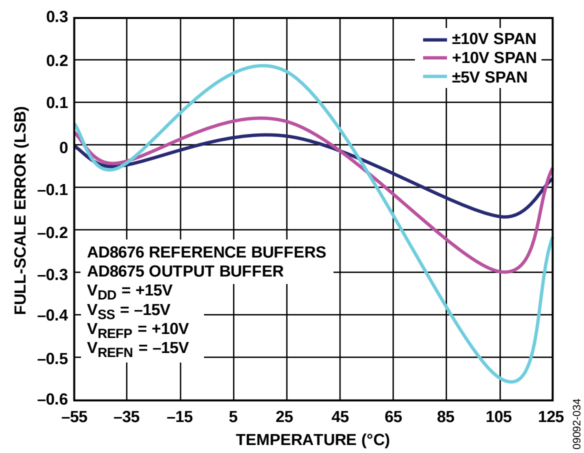


Figure 33. Full-Scale Error vs. Temperature

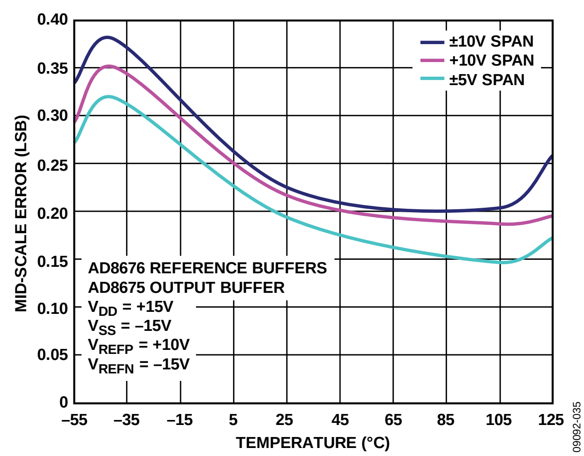


Figure 34. Midscale Error vs. Temperature

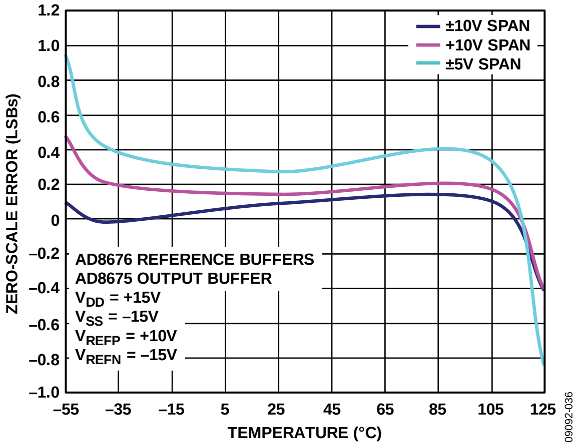


Figure 35. Zero-Scale Error vs. Temperature

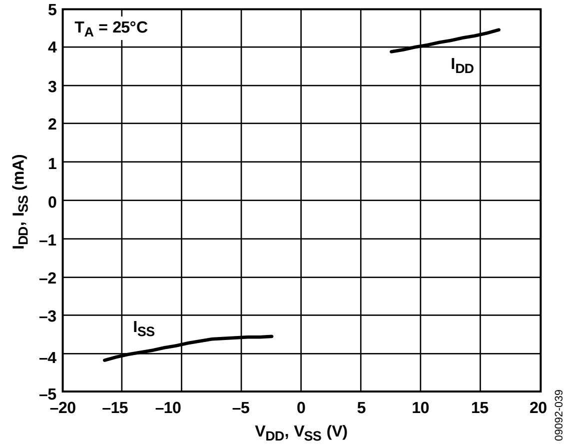


Figure 38. Power Supply Currents vs. Power Supply Voltages

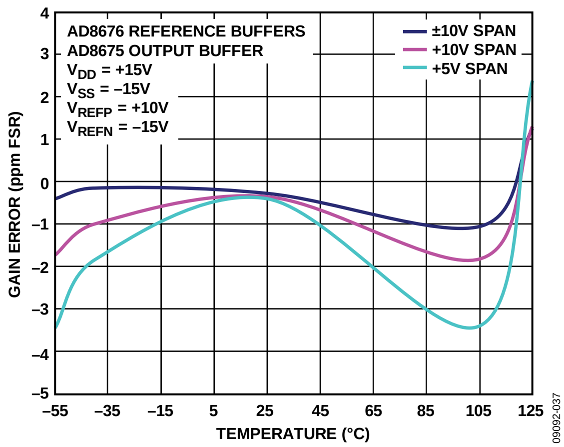


Figure 36. Gain Error vs. Temperature

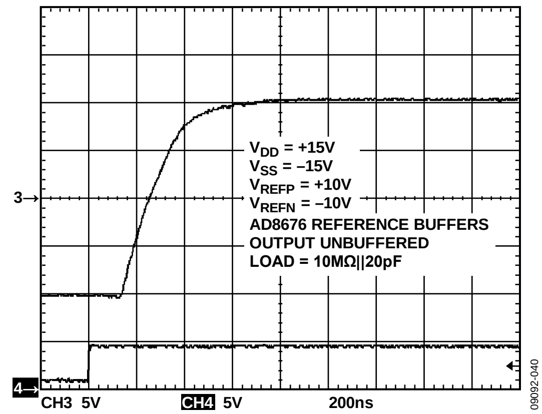


Figure 39. Rising Full-Scale Voltage Step

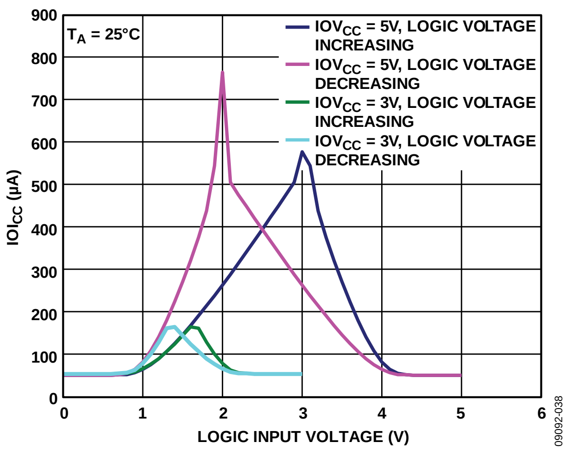


Figure 37. IOI_{CC} vs. Logic Input Voltage

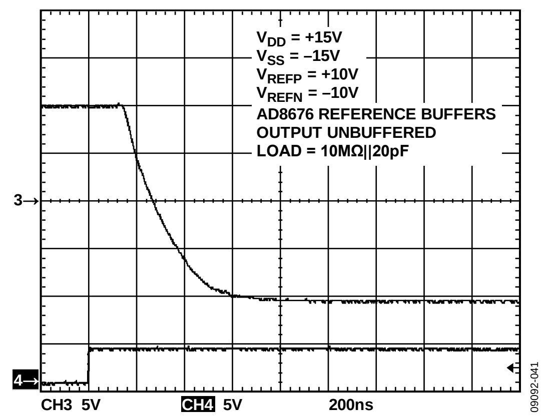


Figure 40. Falling Full-Scale Voltage Step

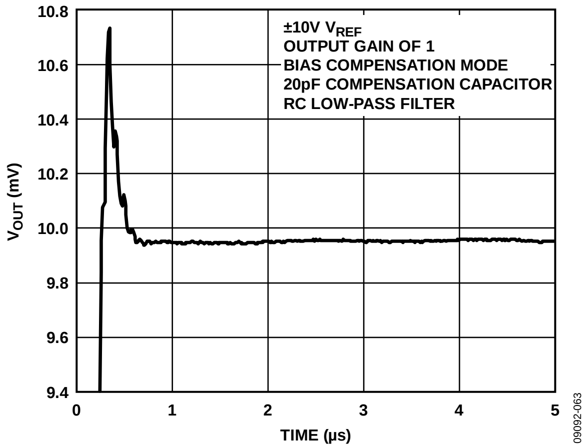


Figure 41. 125 Code Step Settling Time

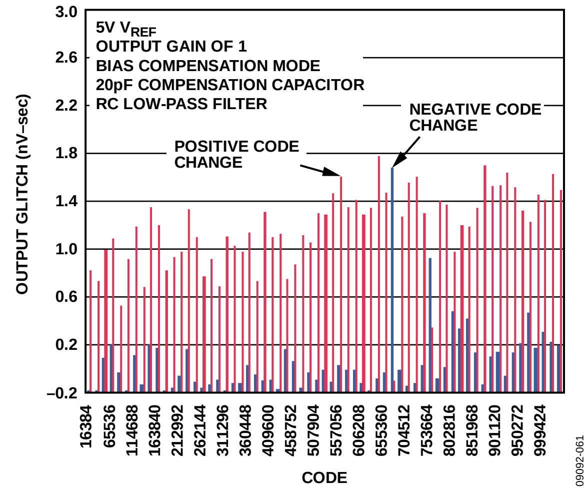


Figure 44. 6 MSB Segment Glitch Energy for 5 V V_{REF}

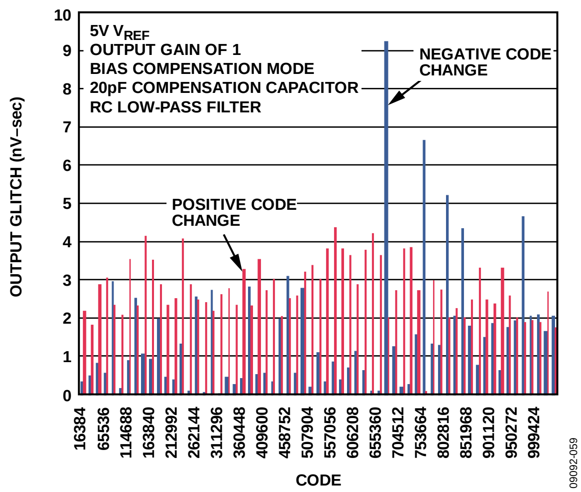


Figure 42. 6 MSB Segment Glitch Energy for ±10 V V_{REF}

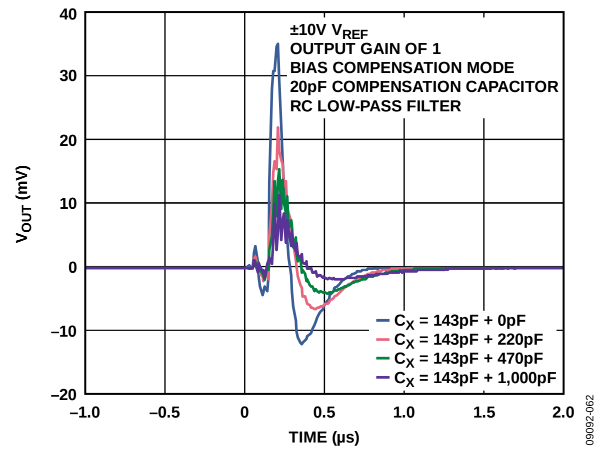


Figure 45. Midscale Peak-to-Peak Glitch for ±10 V

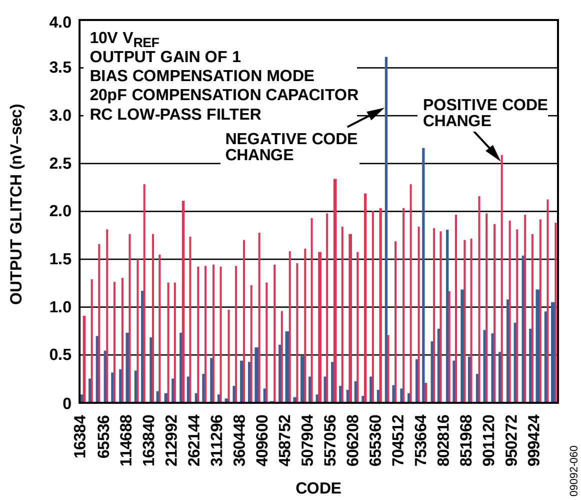


Figure 43. 6 MSB Segment Glitch Energy for 10 V V_{REF}

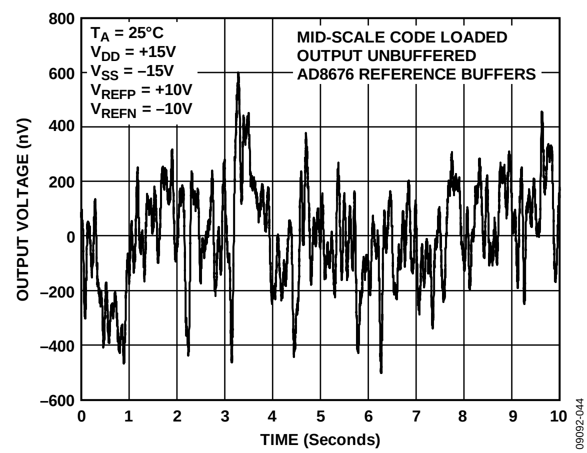


Figure 46. Voltage Output Noise, 0.1 Hz to 10 Hz Bandwidth

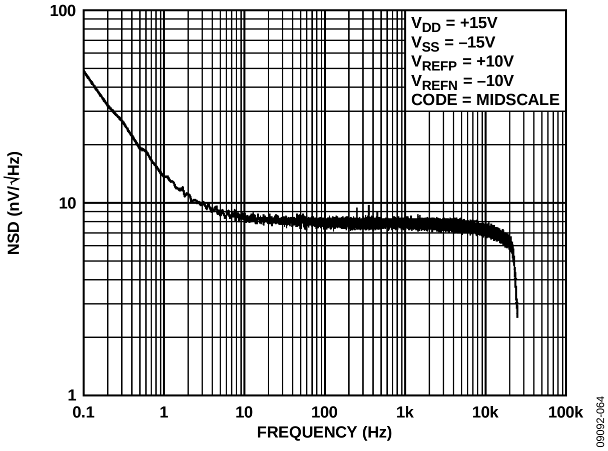


Figure 47. Noise Spectral Density vs. Frequency

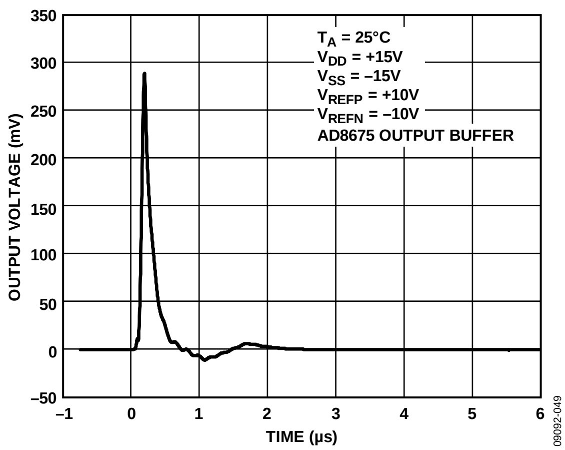


Figure 48. Glitch Impulse on Removal of Output Clamp

TERMINOLOGY

Relative Accuracy

Relative accuracy, or integral nonlinearity (INL), is a measure of the maximum deviation, in LSB, from a straight line passing through the endpoints of the DAC transfer function. A typical INL error vs. code plot is shown in Figure 5.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic. A typical DNL error vs. code plot is shown in Figure 9.

Linearity Error Long-Term Stability

Linearity error long-term stability is a measure of the stability of the linearity of the DAC over a long period of time. It is specified in LSB for a time period of 500 hours and 1000 hours at an elevated ambient temperature.

Zero-Scale Error

Zero-scale error is a measure of the output error when zero-scale code (0x00000) is loaded to the DAC register. Ideally, the output voltage should be V_{REFNS}. Zero-scale error is expressed in LSBs.

Zero-Scale Error Temperature Coefficient

Zero-scale error temperature coefficient is a measure of the change in zero-scale error with a change in temperature. It is expressed in ppm FSR/°C.

Full-Scale Error

Full-scale error is a measure of the output error when full-scale code (0x3FFFF) is loaded to the DAC register. Ideally, the output voltage should be V_{REFPS} − 1 LSB. Full-scale error is expressed in LSBs.

Full-Scale Error Temperature Coefficient

Full-scale error temperature coefficient is a measure of the change in full-scale error with a change in temperature. It is expressed in ppm FSR/°C.

Gain Error

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal, expressed in ppm of the full-scale range.

Gain Error Temperature Coefficient

Gain error temperature coefficient is a measure of the change in gain error with a change in temperature. It is expressed in ppm FSR/°C.

Midscale Error

Midscale error is a measure of the output error when midscale code (0x20000) is loaded to the DAC register. Ideally, the output voltage should be $(V_{REFPS} - V_{REFNS})/2 + V_{REFNS}$. Midscale error is expressed in LSBs.

Midscale Error Temperature Coefficient

Midscale error temperature coefficient is a measure of the change in mid-scale error with a change in temperature. It is expressed in ppm FSR/°C.

Output Slew Rate

Slew rate is a measure of the limitation in the rate of change of the output voltage. The slew rate of the AD5781 output voltage is determined by the capacitive load presented to the V_{OUT} pin. The capacitive load in conjunction with the 3.4 kΩ output impedance of the AD5781 set the slew rate. Slew rate is measured from 10% to 90% of the output voltage change and is expressed in V/µs.

Output Voltage Settling Time

Output voltage settling time is the amount of time it takes for the output voltage to settle to a specified level for a specified change in voltage. For fast settling applications, a high speed buffer amplifier is required to buffer the load from the 3.4 kΩ output impedance of the AD5781, in which case, it is the amplifier that determines the settling time.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition (see Figure 42).

Output Enabled Glitch Impulse

Output enabled glitch impulse is the impulse injected into the analog output when the clamp to ground on the DAC output is removed. It is specified as the area of the glitch in nV-sec (see Figure 48).

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s, and vice versa.

Spurious Free Dynamic Range (SFDR)

Spurious free dynamic range is the usable dynamic range of a DAC before spurious noise interferes or distorts the fundamental signal. It is measured by the difference in amplitude between the fundamental and the largest harmonically or nonharmonically related spur from dc to full Nyquist bandwidth (half the DAC sampling rate, or $f_S/2$). SFDR is measured when the signal is a digitally generated sine wave.

Total Harmonic Distortion (THD)

Total harmonic distortion is the ratio of the rms sum of the harmonics of the DAC output to the fundamental value. Only the second to fifth harmonics are included.

DC Power Supply Rejection Ratio.

DC power supply rejection ratio is a measure of the rejection of the output voltage to dc changes in the power supplies applied to the DAC. It is measured for a given dc change in power supply voltage and is expressed in μV/V.

AC Power Supply Rejection Ratio (AC PSRR)

AC power supply rejection ratio is a measure of the rejection of the output voltage to ac changes in the power supplies applied to the DAC. It is measured for a given amplitude and frequency change in power supply voltage and is expressed in decibels.

THEORY OF OPERATION

The AD5781 is a high accuracy, fast settling, single, 18-bit, serial input, voltage output DAC. It operates from a V_{DD} supply voltage of 7.5 V to 16.5 V and a V_{SS} supply of −16.5 V to −2.5 V. Data is written to the AD5781 in a 24-bit word format via a 3-wire serial interface. The AD5781 incorporates a power-on reset circuit that ensures the DAC output powers up to 0 V with the V_{OUT} pin clamped to AGND through a ~6 kΩ internal resistor.

DAC ARCHITECTURE

The architecture of the AD5781 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 49. The six MSBs of the 18-bit data-word are decoded to drive 63 switches, E0 to E62. Each of these switches connects one of 63 matched resistors to either the V_{REFP} or V_{REFN} voltage. The remaining 12 bits of the data-word drive the S0 to S11 switches of a 12-bit voltage mode R-R ladder network.

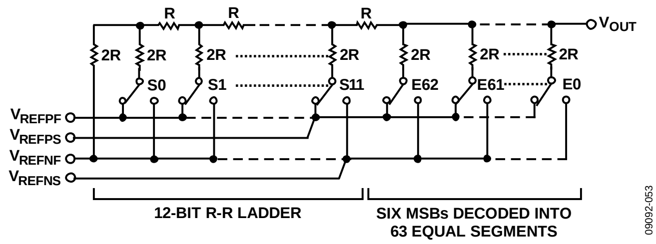


Figure 49. DAC Ladder Structure Serial Interface

The AD5781 has a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and SDIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards, as well as most DSPs (see Figure 2 for a timing diagram).

Input Shift Register

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of a serial clock input, SCLK, which can operate at up to 35 MHz. The input register consists of a R/$\overline{\text{W}}$ bit, three address bits, and twenty data bits as shown in Table 7. The timing diagram for this operation is shown in Figure 2.

Table 7. Input Shift Register Format

MSB					**LSB**
DB23	**DB22**	**DB21**	**DB20**	**DB19**	**DB0**
R/$\overline{\text{W}}$	Register address			Register data	

Table 8. Decoding the Input Shift Register

R/$\overline{\text{W}}$	**Register Address**			**Description**
X[1]	0	0	0	No operation (NOP). Used in readback operations.
0	0	0	1	Write to the DAC register.
0	0	1	0	Write to the control register.
0	0	1	1	Write to the clearcode register.
0	1	0	0	Write to the software control register.
1	0	0	1	Read from the DAC register.
1	0	1	0	Read from the control register.
1	0	1	1	Read from the clearcode register.

[1] X is don't care.

Standalone Operation

The serial interface works with both a continuous and noncontinuous serial clock. A continuous SCLK source can be used only if $\overline{SYNC}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and $\overline{SYNC}$ must be taken high after the final clock to latch the data. The first falling edge of $\overline{SYNC}$ starts the write cycle. Exactly 24 falling clock edges must be applied to SCLK before $\overline{SYNC}$ is brought high again. If $\overline{SYNC}$ is brought high before the 24th falling SCLK edge, the data written is invalid. If more than 24 falling SCLK edges are applied before $\overline{SYNC}$ is brought high, the input data is also invalid. The input shift register is updated on the rising edge of $\overline{SYNC}$. For another serial transfer to take place, $\overline{SYNC}$ must be brought low again. After the end of the serial data transfer, data is automatically transferred from the input shift register to the addressed register. Once the write cycle is complete, the output can be updated by taking $\overline{LDAC}$ low while $\overline{SYNC}$ is high.

Readback

The contents of all the on-chip registers can be read back via the SDO pin. Table 8 outlines how the registers are decoded. After a register has been addressed for a read, the next 24 clock cycles clock the data out on the SDO pin. The clocks must be applied while $\overline{SYNC}$ is low. When $\overline{SYNC}$ is returned high, the SDO pin is placed in tristate. For a read of a single register, the NOP function can be used to clock out the data. Alternatively, if more than one register is to be read, the data of the first register to be addressed can be clocked out at the same time the second register to be read is being addressed. The SDO pin must be enabled to complete a readback operation. The SDO pin is enabled by default.

HARDWARE CONTROL PINS

Load DAC Function ($\overline{LDAC}$)

After data has been transferred into the input register of the DAC, there are two ways to update the DAC register and DAC output. Depending on the status of both $\overline{SYNC}$ and $\overline{LDAC}$, one of two update modes is selected: synchronous DAC updating or asynchronous DAC updating.

Synchronous DAC Update

In this mode, $\overline{LDAC}$ is held low while data is being clocked into the input shift register. The DAC output is updated on the rising edge of $\overline{SYNC}$.

Asynchronous DAC Update

In this mode, $\overline{LDAC}$ is held high while data is being clocked into the input shift register. The DAC output is asynchronously updated by taking $\overline{LDAC}$ low after $\overline{SYNC}$ has been taken high. The update now occurs on the falling edge of $\overline{LDAC}$.

Reset Function ($\overline{RESET}$)

The AD5781 can be reset to its power-on state by two means: either by asserting the $\overline{RESET}$ pin or by utilizing the software RESET control function (see Table 14). If the $\overline{RESET}$ pin is not used, it should be hardwired to IOV_{CC}.

Asynchronous Clear Function (CLR)

The $\overline{CLR}$ pin is an active low clear that allows the output to be cleared to a user defined value. The 18-bit clear code value is programmed to the clearcode register (see Table 13). It is necessary to maintain $\overline{CLR}$ low for a minimum amount of time to complete the operation (see Figure 2). When the $\overline{CLR}$ signal is returned high, the output remains at the clear value (if $\overline{LDAC}$ is high) until a new value is loaded to the DAC register. The output cannot be updated with a new value while the $\overline{CLR}$ pin is low. A clear operation can also be performed by setting the CLR bit in the software control register (see Table 14).

Table 9. Hardware Control Pins Truth Table

$\overline{\text{LDAC}}$	$\overline{\text{CLR}}$	$\overline{\text{RESET}}$	Function
X[1]	X[1]	0	The AD5781 is in reset mode. The device cannot be programmed.
X[1]	X[1]	↑	The AD5781 is returned to its power-on state. All registers are set to their default values.
0	0	1	The DAC register is loaded with the clearcode register value, and the output is set accordingly.
0	1	1	The output is set according to the DAC register value.
1	0	1	The DAC register is loaded with the clearcode register value, and the output is set accordingly.
↓	1	1	The output is set according to the DAC register value.
↓	0	1	The output remains at the clear code value.
↑	1	1	The output remains set according to the DAC register value.
↑	0	1	The output remains at the clear code value.
1	↓	1	The DAC register is loaded with the clearcode register value and the output is set accordingly.
0	↓	1	The DAC register is loaded with the clearcode register value and the output is set accordingly.
1	↑	1	The output remains at the clear code value.
0	↑	1	The output is set according to the DAC register value.

[1] X is don't care.

ON-CHIP REGISTERS

DAC Register

Table 10 outlines how data is written to and read from the DAC register.

Table 10. DAC Register

MSB **LSB**

DB23	DB22	DB21	DB20	DB19	DB2	DB1	DB0
R/$\overline{\text{W}}$	Register address			DAC register data			
R/$\overline{\text{W}}$	0	0	1	18-bits of data		X[1]	X[1]

[1] X is don't care.

The following equation describes the ideal transfer function of the DAC:

$$V_{OUT} = \frac{(V_{REFP} - V_{REFN}) \times D}{2^{18} - 1} + V_{REFN}$$

where:
V_{REFN} is the negative voltage applied at the V_{REFNS} input pin.
V_{REFP} is the positive voltage applied at the V_{REFPS} input pin.
D is the 18-bit code programmed to the DAC.

Control Register

The control register controls the mode of operation of the AD5781.

Table 11. Control Register

MSB															LSB
DB23	**DB22**	**DB21**	**DB20**	**DB19…DB11**	**DB10**	**DB9**	**DB8**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
R/$\overline{W}$	Register address			Control register data											
R/$\overline{W}$	0	1	0	Reserved	Reserved	LIN COMP				SDODIS	BIN/2sC	DACTRI	OPGND	RBUF	Reserved

Table 12. Control Register Functions

Function	Description
Reserved	These bits are reserved and should be programmed to zero.
RBUF	Output amplifier configuration control. 0: internal amplifier, A1, is powered up and resistors RFB and R1 are connected in series as shown in Figure 52. This allows an external amplifier to be connected in a gain of two configurations. See the AD5781 Features section for further details. 1: (default) internal amplifier, A1, is powered down and resistors RFB and R1 are connected in parallel as shown in Figure 51 so that the resistance between the RFB and INV pins is 3.4 kΩ, equal to the resistance of the DAC. This allows the RFB and INV pins to be used for input bias current compensation for an external unity gain amplifier. See the AD5781 Features section for further details.
OPGND	Output ground clamp control. 0: DAC output clamp to ground is removed, and the DAC is placed in normal mode. 1: (default) DAC output is clamped to ground through a ~6 kΩ resistance, and the DAC is placed in tristate mode. Resetting the part puts the DAC in OPGND mode, where the output ground clamp is enabled and the DAC is tristated. Setting the OPGND bit to 1 in the control register overrules any write to the DACTRI bit
DACTRI	DAC tristate control. 0: DAC is in normal operating mode. 1: (default) DAC is in tristate mode.
BIN/2sC	DAC register coding select. 0: (default) DAC register uses twos complement coding. 1: DAC register uses offset binary coding.
SDODIS	SDO pin enable/disable control. 0: (default) SDO pin is enabled. 1: SDO pin is disabled (tristate).
LIN COMP	Linearity error compensation for varying reference input spans. See the AD5781 Features section for further details.
	0 0 0 0 (Default) reference input span up to 10 V.
	1 1 0 0 Reference input span of 20 V.

Clearcode Register

The clearcode register sets the value to which the DAC output is set when the $\overline{\text{CLR}}$ pin or CLR bit is asserted. The output value depends on the DAC coding that is being used, either binary or twos complement. The default register value is 0.

Table 13. Clearcode Register

MSB							LSB
DB23	**DB22**	**DB21**	**DB20**	**DB19**	**DB2**	**DB1**	**DB0**
R/$\overline{W}$	Register address			Clearcode register data			
R/$\overline{W}$	0	1	1	18-bits of data		X[1]	X[1]

[1] X is don't care.

Software Control Register

This is a write only register in which writing a 1 to a particular bit has the same effect as pulsing the corresponding pin low.

Table 14. Software Control Register

MSB **LSB**

DB23	DB22	DB21	DB20	DB19	DB3	DB2	DB1	DB0
R/$\overline{W}$	Register address			Software control register data				
0	1	0	0	Reserved		RESET	CLR[1]	LDAC[2]

[1] The CLR function has no effect if the $\overline{LDAC}$ pin is low.
[2] The LDAC function has no effect if the $\overline{CLR}$ pin is low.

Table 15. Software Control Register Functions

Function	Description
LDAC	Setting this bit to 1 updates the DAC register and consequently the DAC output.
CLR	Setting this bit to 1 sets the DAC register to a user defined value (see Table 13) and updates the DAC output. The output value depends on the DAC register coding that is being used, either binary or twos complement.
RESET	Setting this bit to 1 returns the AD5781 to its power-on state.

AD5781 FEATURES

POWER-ON TO 0 V

The AD5781 contains a power-on reset circuit that, as well as resetting all registers to their default values, controls the output voltage during power-up. Upon power-on, the DAC is placed in tristate (its reference inputs are disconnected), and its output is clamped to AGND through a ~6 kΩ resistor. The DAC remains in this state until programmed otherwise via the control register. This is a useful feature in applications where it is important to know the state of the DAC output while it is in the process of powering up.

CONFIGURING THE AD5781

After power-on, the AD5781 must be configured to put it into normal operating mode before programming the output. To do this, the control register must be programmed. The DAC is removed from tristate by clearing the DACTRI bit, and the output clamp is removed by clearing the OPGND bit. At this point, the output goes to V_{REFN} unless an alternative value is first programmed to the DAC register.

DAC OUTPUT STATE

The DAC output can be placed in one of three states, controlled by the DACTRI and OPGND bits of the control register, as shown in Table 16.

Table 16. AD5781 Output State Truth Table

DACTRI	OPGND	Output State
0	0	Normal operating mode.
0	1	Output is clamped via ~6 kΩ to AGND.
1	0	Output is in tristate.
1	1	Output is clamped via ~6 kΩ to AGND.

LINEARITY COMPENSATION

The integral nonlinearity (INL) of the AD5781 can vary according to the applied reference voltage span; the LIN COMP bits of the control register can be programmed to compensate for this variation in INL. The specifications in this data sheet are obtained with LIN COMP = 0000 for reference spans up to and including 10 V and with LIN COMP = 1100 for a reference span of 20 V. The default value of the LIN COMP bits is 0000.

OUTPUT AMPLIFIER CONFIGURATION

There are a number of different ways that an output amplifier can be connected to the AD5781, depending on the voltage references applied and the desired output voltage span.

Unity Gain Configuration

Figure 50 shows an output amplifier configured for unity gain, in this configuration the output spans from V_{REFN} to V_{REFP}.

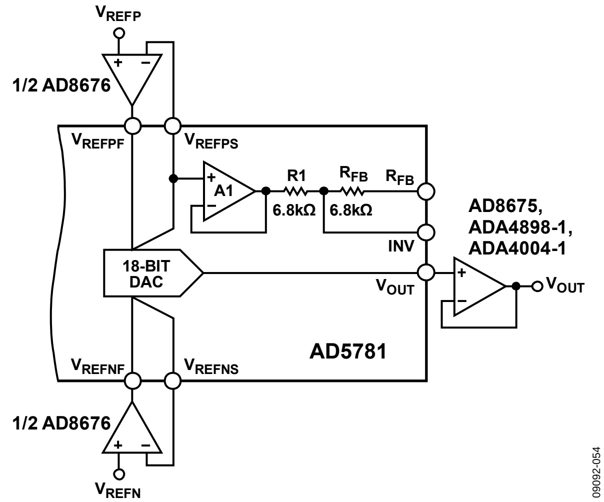


Figure 50. Output Amplifier in Unity Gain Configuration

A second unity gain configuration for the output amplifier is one that removes an offset from the input bias currents of the amplifier. It does this by inserting a resistance in the feedback path of the amplifier that is equal to the output resistance of the DAC. The DAC output resistance is 3.4 kΩ. By connecting R1 and R_{FB} in parallel, a resistance equal to the DAC resistance is available on-chip. Because the resistors are all on one piece of silicon, they are temperature coefficient matched. To enable this mode of operation, the RBUF bit of the control register must be set to Logic 1. Figure 51 shows how the output amplifier is connected to the AD5781. In this configuration, the output amplifier is in unity gain and the output spans from V_{REFN} to V_{REFP}. This unity gain configuration allows a capacitor to be placed in the amplifier feedback path to improve dynamic performance.

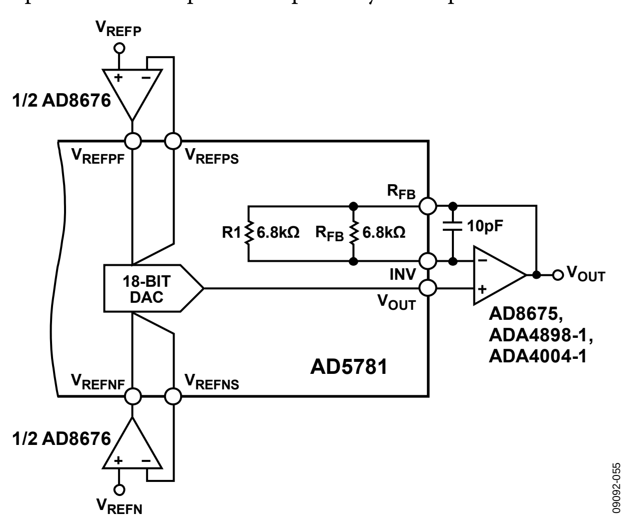


Figure 51. Output Amplifier in Unity Gain with Amplifier Input Bias Current Compensation

Gain of Two Configuration

Figure 52 shows an output amplifier configured for a gain of two. The gain is set by the internal matched 6.8 kΩ resistors, which are exactly twice the DAC resistance, having the effect of removing an offset from the input bias current of the external amplifier. In this configuration, the output spans from 2 × V_{REFN} − V_{REFP} to V_{REFP}. This configuration is used to generate a bipolar output span from a single-ended reference input, with V_{REFN} = 0 V. For this mode of operation, the RBUF bit of the control register must be cleared to Logic 0.

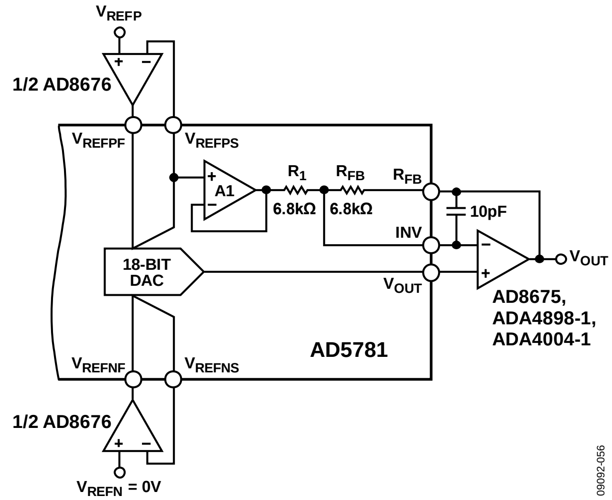


Figure 52. Output Amplifier in Gain of Two Configuration

APPLICATIONS INFORMATION

TYPICAL OPERATING CIRCUIT

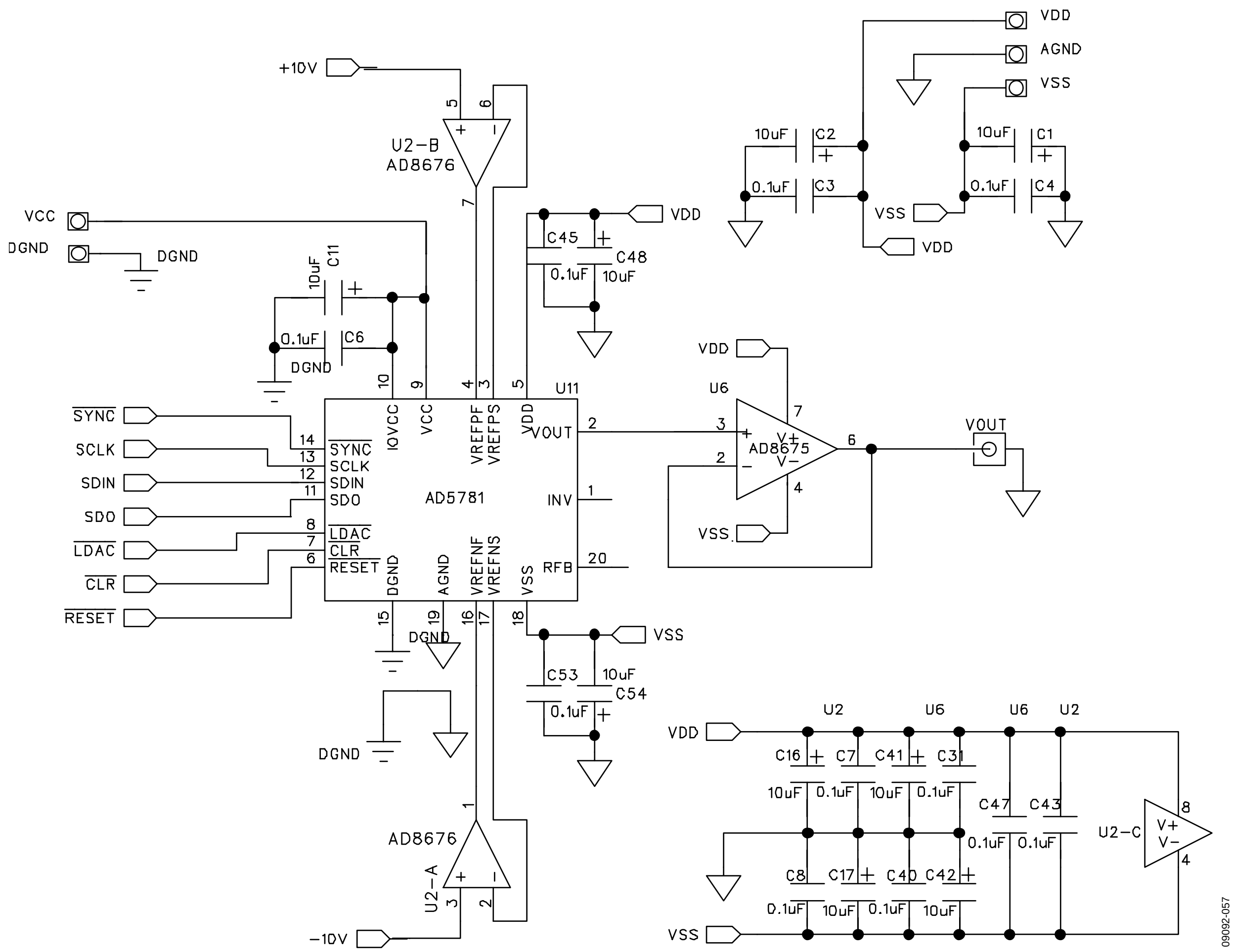


Figure 53. Typical Operating Circuit

Figure 53 shows a typical operating circuit for the AD5781 using an AD8676 for reference buffers and an AD8675 as an output buffer. To meet the specified linearity, force sense buffers must be used on the reference inputs. Because the output impedance of the AD5781 is 3.4 kΩ, an output buffer is required for driving low resistive, high capacitive loads.

EVALUATION BOARD

An evaluation board is available for the AD5781 to aid designers in evaluating the high performance of the part with minimum effort. The AD5781 evaluation kit includes a populated and tested AD5781 PCB. The evaluation board interfaces to the USB port of a PC. Software is available with the evaluation board to allow the user to easily program the AD5781. The software runs on any PC that has Microsoft® Windows® XP (SP2) or Vista (32 bits) installed. The EVAL-AD5781 data sheet is available, which gives full details on the operation of the evaluation board

OUTLINE DIMENSIONS

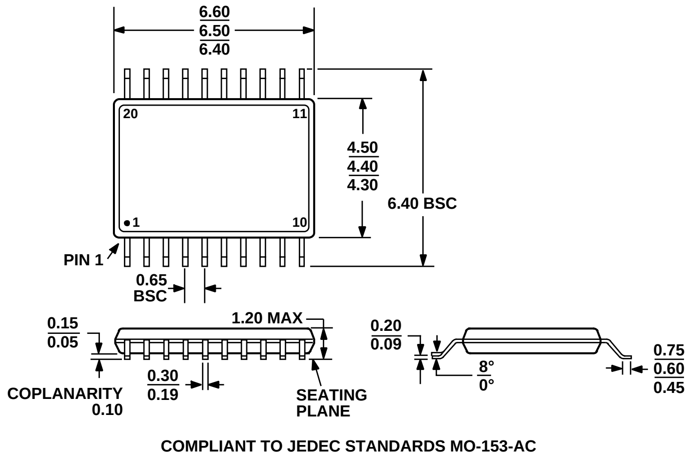


Figure 54. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	INL	Package Description	Package Option
AD5781BRUZ	−40°C to +125°C	±0.5 LSB	20-Lead TSSOP	RU-20
AD5781BRUZ-REEL7	−40°C to +125°C	±0.5 LSB	20-Lead TSSOP	RU-20
AD5781ARUZ	−40°C to +125°C	±4 LSB	20-Lead TSSOP	RU-20
AD5781ARUZ-REEL7	−40°C to +125°C	±4 LSB	20-Lead TSSOP	RU-20
EVAL-AD5781SDZ			Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES