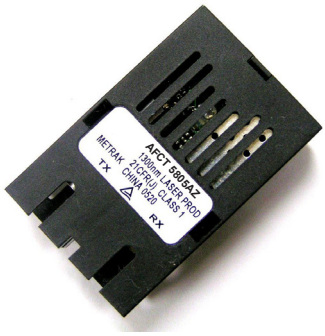
AFCT-5805xxxZ

155 Mb/s Single Mode Fiber Optic Transceiver
for ATM, SONET OC-3/SDH STM-1

Data Sheet



Description

General

The AFCT-5805xxxZ transceiver is a high performance, cost effective module for serial optical data communications applications specified for a data rate of 155 Mb/s. It is designed to provide a SONET/SDH compliant link for intermediate reach links operating at +3.3 V or +5.0 V input voltage.

Transmitter Section

The transmitter section of the AFCT-5805xxxZ consists of a 1300 nm FP laser in an eyesafe optical subassembly (OSA) which mates to the fiber cable. The laser OSA is driven by a custom IC which converts differential input PECL logic signals, ECL referenced (shifted) to +3.3 V or +5 V supply, into an analog laser drive current.

Receiver Section

The receiver utilizes an InGaAs PIN photodiode mounted together with a transimpedance preamplifier IC in an OSA. This OSA is connected to a circuit providing post- amplification quantization, and optical signal detection.

Features

- 1300 nm Single mode transceiver for links up to 15 Km
- Compliant with T1.646-1995 Broadband ISDN and T1E1.2/98-011R1 SONET network to customer installation interface standards
- Compliant with T1.105.06 SONET physical layer specifications standard
- Multisourced 1 x 9 pin configuration
- Can replace LED multisourced 1 x 9 transceivers
- Unconditionally eyesafe laser IEC 825/CDRH Class 1 compliant
- Integral duplex SC connector receptacle compatible with TIA/EIA and IEC standards.
- RoHS compliant
- Two Temperature Ranges:
  AFCT-5805BZ/DZ 0°C to +70°C
  AFCT-5805AZ/CZ -40°C to +85°C
  AFCT-5805AMZ -40°C to +85°C
  AFCT-5805AEMZ -40°C to +85°C
- Single +3.3 V or +5.0 V power supply operation
- Wave solder and aqueous wash process compatible
- Manufactured in an ISO 9002 certified facility
- Considerable EMI margin to FCC Class B

Applications

- ATM 155 Mb/s links for LAN backbone switches and routers
- ATM 155 Mb/s links for WAN core, edge and access switches and routers
- ATM 155 Mb/s links for add/drop multiplexers and demultiplexers
- SONET OC-3/SDH STM-1 (S-1.1) interconnections

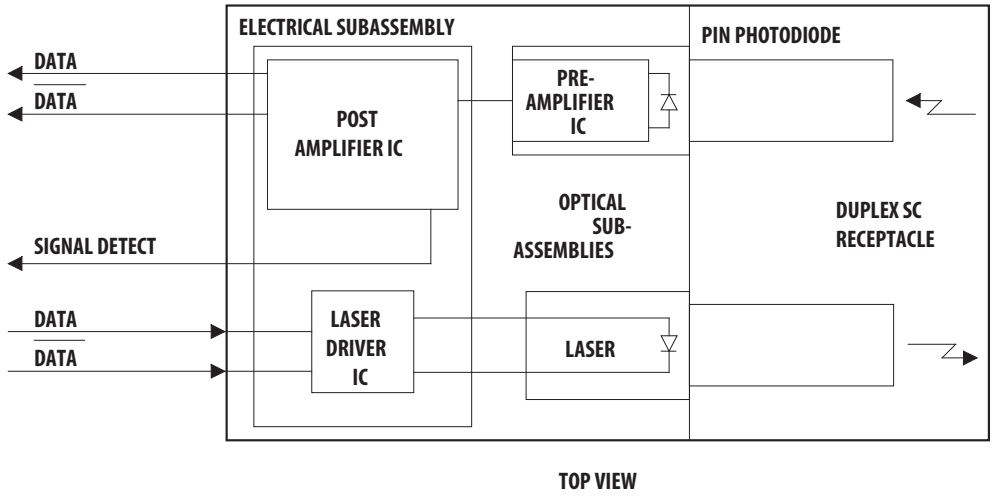


Figure 1. Block Diagram

Receiver Signal Detect

Signal Detect is a basic fiber failure indicator. This is a single-ended PECL output. As the input optical power is decreased, Signal Detect will switch from high to low (deassert point) somewhere between sensitivity and the no light input level. As the input optical power is increased from very low levels, Signal Detect will switch back from low to high (assert point). The assert level will be at least 0.5 dB higher than the deassert level.

Transceiver Specified for Wide Temperature Range Operation

The AFCT-5805xxxZ is specified for operation over extended temperature range of -40° to +85°C.

Characterization of the parts has been performed over the ambient operating temperature range in an airflow of 2 m/s.

Other Members of Avago Technologies SC Duplex 155 Mb/s Product Family

- HFCT-5801, 1300 nm single mode transceiver for links up to 15 km. The part is based on the 2 x 9 industry standard package and has laser bias, optical power monitor and transmitter disable functions.

Applications Information

Typical BER Performance of Receiver versus Input Optical Power Level

The AFCT-5805xxxZ transceiver can be operated at Bit-Error-Rate conditions other than the required BER = 1 x 10^{-10} of the ATM Forum 155.52 Mb/s Physical Layer Standard. The typical trade-off of BER versus Relative Input Optical Power is shown in Figure 2. The Relative Input Optical Power in dB is referenced to the actual sensitivity of the device. For BER conditions better than 1 x 10^{-10}, more input signal is needed (+dB).

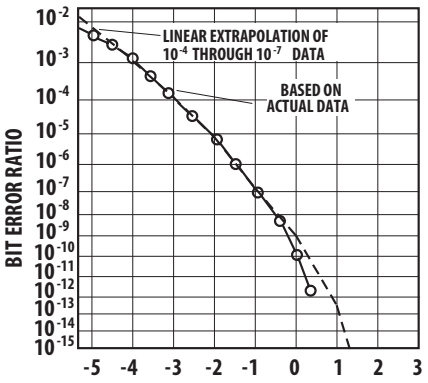


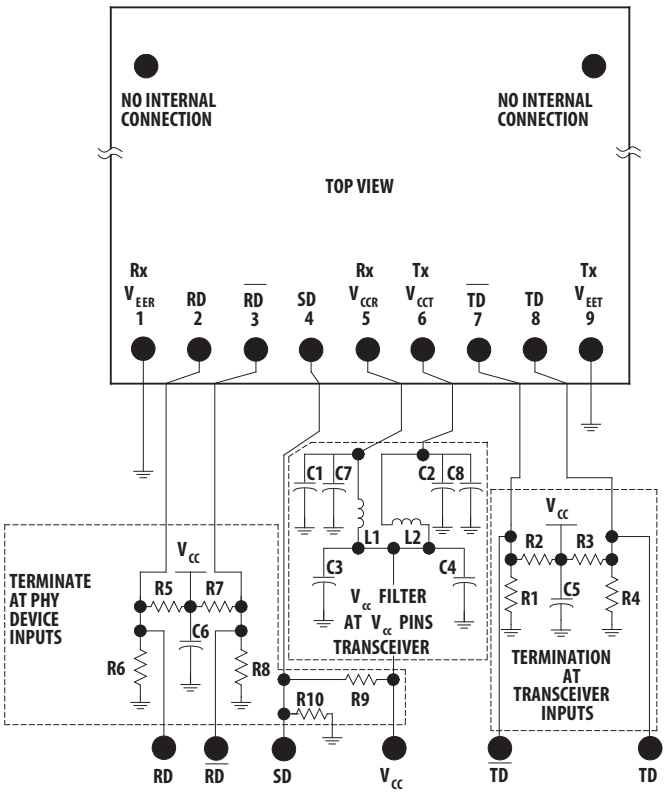
Figure 2. Relative Input Optical Power - dBm. Avg.

Recommended Circuit Schematic

In order to ensure proper functionality of the AFCT-5805xxxZ a recommended circuit is provided in Figure 3. When designing the circuit interface, there are a few fundamental guidelines to follow. For example, in the Recommended Circuit Schematic figure the differential data lines should be treated as 50 ohm Microstrip or stripline transmission lines. This will help to minimize the parasitic inductance and capacitance effects. Proper termination of the differential data signals will prevent reflections and ringing which would compromise the signal fidelity and generate unwanted electrical noise. Locate termination at the received signal end of the transmission line. The length of these lines should be kept short and of equal length. For the high speed signal lines, differential signals should be used, not single-ended signals, and these differential signals need to be loaded symmetrically to prevent unbalanced currents from flowing which will cause distortion in the signal.

Maintain a solid, low inductance ground plane for returning signal currents to the power supply. Multilayer plane printed circuit board is best for distribution of V_{CC}, returning ground currents, forming transmission lines and shielding, Also, it is important to suppress noise from influencing the fiber-optic transceiver performance, especially the receiver circuit. Proper power supply filtering of V_{CC} for this transceiver is accomplished by using the recommended, separate filter circuits shown in Figure 3 for the transmitter and receiver sections. These filter circuits suppress V_{CC} noise over a broad frequency range, this prevents receiver sensitivity degradation due to V_{CC} noise. It is recommended that surface-mount components be used. Use tantalum capacitors for the 10 µF capacitors and monolithic, ceramic bypass capacitors for the 0.1 µF capacitors. Also, it is recommended that a surface- mount coil inductor of 3.3 µH be used. Ferrite beads can be used to replace the coil inductors when using quieter V_{CC} supplies, but a coil inductor is recommended over a ferrite bead. All power supply components need to be placed physically next to the V_{CC} pins of the receiver and transmitter. Use a good, uniform ground plane with a minimum number of holes to provide a low-inductance ground current return for the power supply currents.

In addition to these recommendations, Avago Technologies Application Engineering staff is available for consulting on best layout practices with various vendors mux/demux, clock generator and clock recovery circuits. Avago Technologies has participated in several reference design studies and is prepared to share the findings of these studies with interested customers. Contact your local Avago Technologies sales representative to arrange for this service.



NOTES:
THE SPLIT-LOAD TERMINATIONS FOR PECL SIGNALS NEED TO BE LOCATED AT THE INPUT OF DEVICES RECEIVING THOSE PECL SIGNALS.
RECOMMEND 4-LAYER PRINTED CIRCUIT BOARD WITH 50 Ω MICROSTRIP SIGNAL PATHS BE USED.

FOR +5.0V AND +3.3V OPERATION.
R1 = R4 = R6 = R8 = R10 = 130 Ω
R2 = R3 = R5 = R7 = R9 = 82 Ω
C1 = C2 = 10 µF
C3 = C4 = C7 = C8 = 100 nF
C5 = C6 = 0.1 µF
L1 = L2 = 3.3 µH COIL OR FERRITE INDUCTOR.

Figure 3. Recommended Circuit Schematic

Evaluation Circuit Boards

Evaluation circuit boards are available from Avago Technologies Application Engineering staff. Contact your local Avago Technologies sales representative to arrange for access to one if needed.

Recommended Solder Fluxes and Cleaning/Degreasing Chemicals

Solder fluxes used with the AFCT-5805xxxZ fiber-optic transceiver should be water-soluble, organic solder fluxes. Some recommended solder fluxes are Lonco 3355-11 from London Chemical West, Inc. of Burbank, CA, and 100 Flux from Alpha Metals of Jersey City, NJ.

Recommended cleaning and degreasing chemicals for the AFCT-5805xxxZ are alcohol's (methyl, isopropyl, isobutyl), aliphatics (hexane, heptane) and other chemicals, such as soap solution or naphtha. Do not use partially halogenated hydrocarbons for cleaning/degreasing. Examples of chemicals to avoid are 1.1.1. trichloroethane, ketones (such as MEK), acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride or N-methylpyrrolidone.

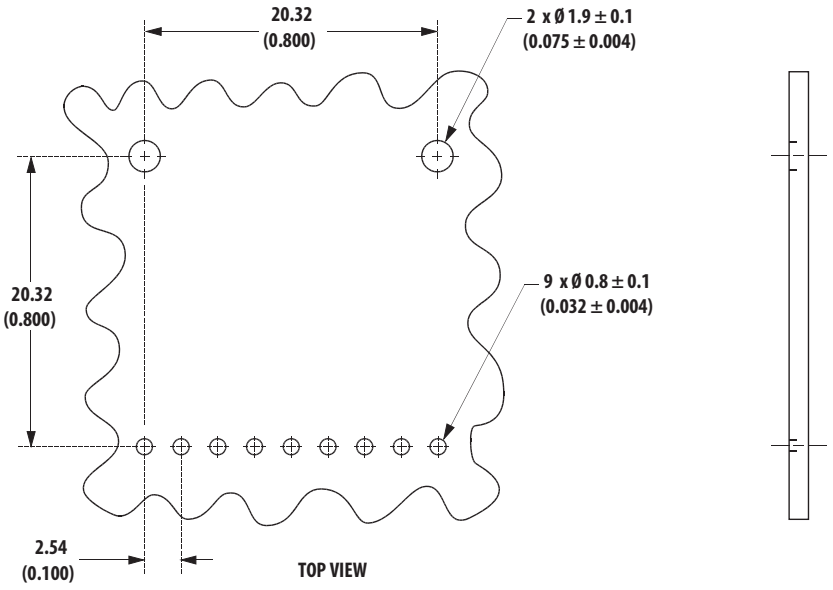
Recommended Solder and Wash Process

The AFCT-5805xxxZ is compatible with industry standard wave or hand solder processes.

A drying cycle must be completed after wash process to remove all moisture from the module.

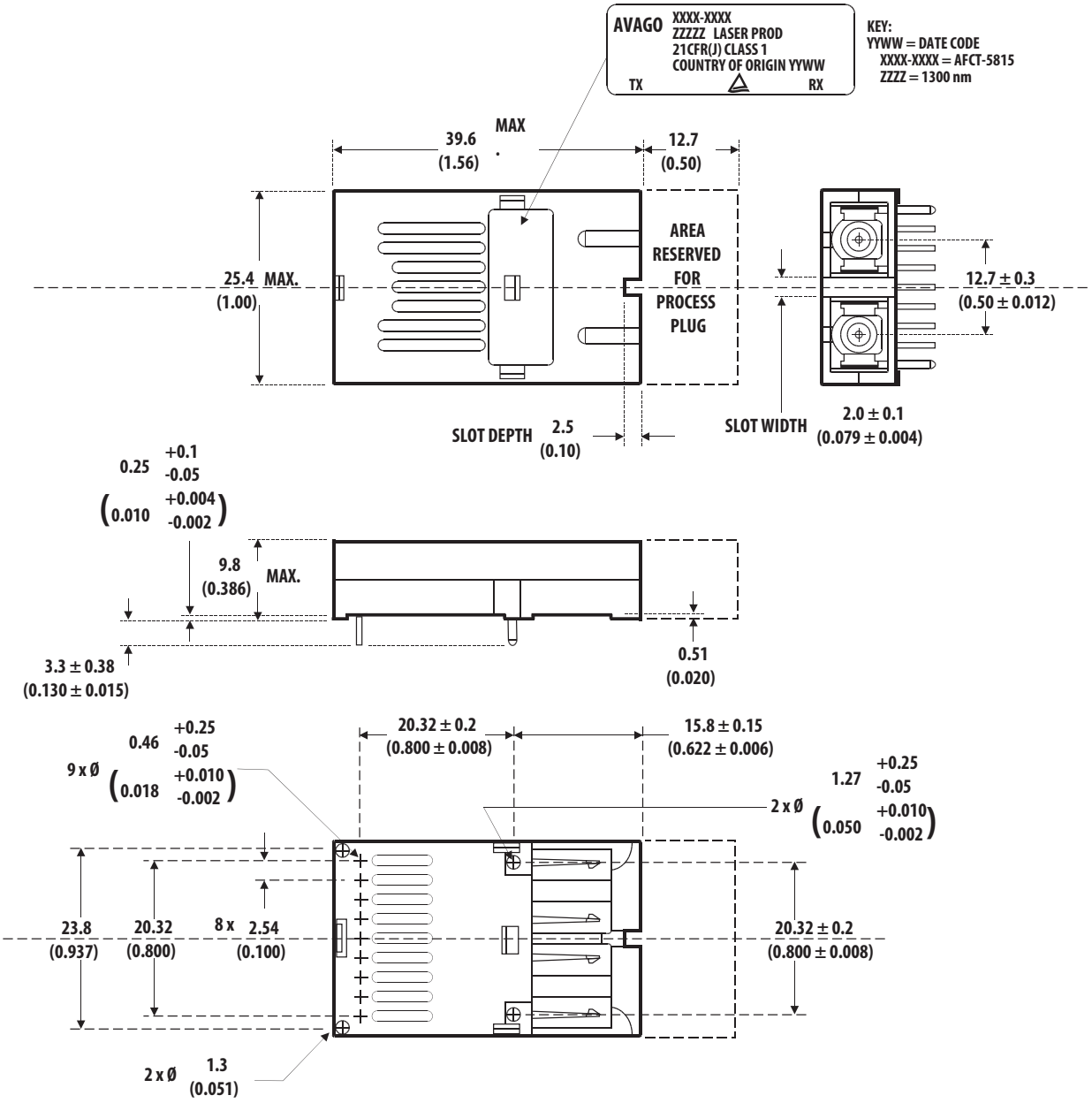
AFCT-5805xxxZ Process Plug

The AFCT-5805xxxZ transceiver is supplied with a process plug for protection of the optical ports with the Duplex SC connector receptacle. This process plug prevents contamination during wave solder and aqueous rinse as well as during handling, shipping or storage. Each process plug can only be used once during processing, although with subsequent use, it can be used as a dust cover. It is made of high-temperature, molded, sealing material that will withstand +85°C and a rinse pressure of 110 lb/in^2.



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Figure 4. Recommended Board Layout Hole Pattern



DIMENSIONS ARE IN MILLIMETERS (INCHES).
TOLERANCES: ±0.1 mm UNLESS OTHERWISE SPECIFIED.

Figure 5. Package Outline Drawing and Pinout

Regulatory Compliance

The AFCT-5805xxxZ is intended to enable commercial system designers to develop equipment that complies with the various regulations governing certification of Information Technology Equipment. See the Regulatory Compliance Table 1 for details. Additional information is available from your Avago Technologies sales representative.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches and floor mats in ESD controlled areas.

The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the duplex SC connector is exposed to the outside of the equipment chassis it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high-speed transceivers from Avago Technologies will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

The AFCT-5805xxxZ has been characterized without a chassis enclosure to demonstrate the robustness of the part's integral shielding. Performance of a system containing these transceivers within a well designed chassis is expected to be better than the results of these tests with no chassis enclosure.

Immunity

Equipment utilizing these AFCT-5805xxxZ transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers, with their integral shields, have been characterized without the benefit of a normal equipment chassis enclosure and the results are reported below. Performance of a system containing these transceivers within a well designed chassis is expected to be better than the results of these tests without a chassis enclosure.

Table 1. Regulatory Compliance - Typical Performance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MII-STD-883F Method 3015.7	Class 1 (>500 V) - Human Body Model
Electrostatic Discharge (ESD) to the Duplex SC Receptacle	Variation of IEC 61000-4-2	Air discharge 15 kV
Electromagnetic Interference (EMI)	FCC Class B	Typically provide greater than 11 dB margin below 1 GHz to FCC Class B when tested in a GTEM with the transceiver mounted to a circuit card without a chassis enclosure at frequencies up to 1 GHz. Margins above 1 GHz dependent on customer board and chassis designs.
Immunity	Variation of IEC 801-3	Typically show no measurable effect from a 10 V/m field swept from 27 MHz to 1 GHz applied to the transceiver without a chassis enclosure.
Eye Safety	FDA CDRH 21-CFR 1040 Class 1	Accession Number: 9521220-121
	IEC 60825 - 1	TUV Approved
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment Including Electrical	UL File#: E173874

Performance Specifications

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	+85	°C	
Lead Soldering Temperature/Time	-	-	+260/10	°C/s	
Input Voltage	-	GND	V_{CC}	V	
Power Supply Voltage	-	0	6	V	

Operating Environment

Parameter	Symbol	Minimum	Maximum	Units	Notes
Power Supply Voltage	V_{CC}	+3.1	+5.25	V	
Ambient Operating Temperature - AFCT-5805AZ/CZ/AMZ	T_{OP}	-40	+85	°C	1
Ambient Operating Temperature - AFCT-5805BZ/DZ	T_{OP}	0	+70	°C	1

Transmitter Section

(Ambient Operating Temperature, V_{CC} = 3.1 V to 5.25 V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Output Center Wavelength	lce	1261	-	1360		
Output Spectral Width (RMS)	Dl	-	-	7.7	nm	
Average Optical Output Power	P_O	-15	-	-8	dBm	2
Extinction Ratio	E_R	8.2	-	-	dB	
Power Supply Current	I_{CC}	-	50	140	mA	3
Output Eye	Compliant with Telcordia TR-NWT-000253 and ITU recommendation G.957					
Optical Rise Time	t_R	-	-	2	ns	4
Optical Fall Time	t_F	-	-	2	ns	4
Data Input Current - Low	I_{IL}	-350	-	-	µA	
Data Input Current - High	I_{IH}	-	-	350	µA	
Data Input Voltage - Low	V_{IL} - V_{CC}	-2.0	-	-1.475	V	5
Data Input Voltage - High	V_{IH} - V_{CC}	-1.165	-	-0.74	V	5

Notes:

1. 2 m/s air flow required.
2. Output power is power coupled into a single mode fiber.
3. The power supply current varies with temperature. Maximum current is specified at V_{CC} = Maximum @ maximum temperature (not including terminations) and end of life. Typical power supply current at +25°C and +3.3 V or +5.0 V supply.
4. 10% - 90% Values. Maximum t_R, t_F times tested against eye mask.
5. These inputs are compatible with 10 K, 10 KH and 100 K PECL outputs.

Receiver Section

(Ambient Operating Temperature, V_{CC} = 3.1 V to 5.25 V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Receiver Sensitivity	-	-	-	-31	dBm	6
Maximum Input Power	-	-7	-	-	dBm	6
Power Supply Current	I_{CC}	-	55	100	mA	7
Signal Detect - Deasserted	-	-45	-	-31	dBm	
Signal Detect - Hysteresis	-	0.5	-	4	dB	
Signal Detect Assert Time (off to on)	AS_Max	-	-	100	µs	
Signal Detect Deassert Time (on to off)	ANS_Max	-	-	350	µs	
Signal Detect Output Voltage - Low	V_{OL} - V_{CC}	-1.92	-	-1.45	V	8
Signal Detect Output Voltage - High	V_{OH} - V_{CC}	-1.1	-	-0.85	V	8
Data Output Voltage - Low	V_{OL} - V_{CC}	-2.0	-	-1.45	V	8
Data Output Voltage - High	V_{OH} - V_{CC}	-1.1	-	-0.85	V	8
Data Output Rise Time	t_r	-	-	2.2	ns	9
Data Output Fall Time	t_f	-	-	2.2	ns	9

Notes

6. Sensitivity and maximum input power levels for a 2^{23}-1 PRBS with 72 ones and 72 zeros inserted. (ITU recommendation G.958).
7. The current includes capacitively coupled 50 Ohm terminations.
8. These outputs are compatible with 10 K, 10 KH and 100 K PECL outputs.
9. 20 - 80% levels.

Table 2. Pin Out Table

Pin	Symbol	Functional Description
Mounting Studs		The mounting studs are provided for transceiver mechanical attachment to the circuit board. They are embedded in the housing and are not connected to the transceiver internal circuit. They should be soldered into plated-through holes on the printed circuit board.
1	V_{EER}	Receiver Signal Ground Directly connect this pin to receiver signal ground plane.
2	RD+	Receiver Data Out Terminate this high-speed, differential, PECL output with standard PECL techniques at the follow-on device input pin.
3	RD-	Receiver Data Out Bar Terminate this high-speed, differential, PECL output with standard PECL techniques at the follow-on device input pin.
4	SD	Signal Detect Normal input optical levels to the receiver result in a logic "1" output. Low input optical levels to the receiver result in a fault indication shown by a logic "0" output. Signal Detect is a single-ended, PECL output. This output will operate with 270 Ω termination resistor to V_{EE} to achieve PECL output levels. This Signal Detect output can be used to drive a PECL input on an upstream circuit, such as, Signal Detect input and Loss of Signal-bar input.
5	V_{CCR}	Receiver Power Supply Provide +3.3 or +5.0 V dc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCR} pin.
6	V_{CCT}	Transmitter Power Supply Provide +3.3 or +5.0 V dc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCT} pin.
7	TD-	Transmitter Data In Bar Terminate this high-speed, differential Transmitter Data input with standard PECL techniques at the transmitter input pin.
8	TD+	Transmitter Data In Terminate this high-speed, differential Transmitter Data input with standard PECL techniques at the transmitter input pin.
9	V_{EET}	Transmitter Signal Ground Directly connect this pin to the transmitter signal ground plane.

Order Information:

Temperature Range 0°C to +70°C

AFCT-5805BZ	Black Case
AFCT-5805DZ	Blue Case

Temperature Range -40°C to +85°C

AFCT-5805AZ	Black Case
AFCT-5805CZ	Blue Case
AFCT-5805AMZ	Metalized Housing
AFCT-5805AEMZ	Metalized Housing with E-shield

Class 1 Laser Product: This product conforms to the applicable requirements of 21 CFR 1040 at the date of manufacture

Date of Manufacture: _____

Avago Technologies Inc., No 1 Yishun Ave 7, Singapore

Handling Precautions

1. The AFCT-5805xxxZ can be damaged by current surges or overvoltage. Power supply transient precautions should be taken.
2. Normal handling precautions for electrostatic sensitive devices should be taken.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

Avago, Avago Technologies, and the A logo are trademarks of Avago Technologies in the United States and other countries.
Data subject to change. Copyright © 2005-2014 Avago Technologies. All rights reserved. Obsoletes AV01-0034EN
AV02-0807EN - December 9, 2014