



# MICROCHIP

# MCP23008/MCP23S08

## 8-Bit I/O Expander with Serial Interface

### Features

- 8-Bit remote bidirectional I/O port
  - I/O pins default to input
- High-speed I<sup>2</sup>C™ interface (**MCP23008**)
  - 100 kHz
  - 400 kHz
  - 1.7 MHz
- High-speed SPI™ interface (**MCP23S08**)
  - 10 MHz
- Hardware address pins
  - Three for the MCP23008 to allow up to eight devices on the bus
  - Two for the MCP23S08 to allow up to four devices using the same chip select
- Configurable interrupt output pin
  - Configurable as active-high, active-low or open-drain
- Configurable interrupt source
  - Interrupt-on-change from configured defaults or pin change
- Polarity inversion register to configure the polarity of the input port data
- External reset input
- Low standby current: 1 µA (max.)
- Operating voltage:
  - 1.8V to 5.5V @ -40°C to +85°C (I-Temp)
  - 2.7V to 5.5V @ -40°C to +85°C (I-Temp)
  - 4.5V to 5.5V @ -40°C to +125°C (E-Temp)

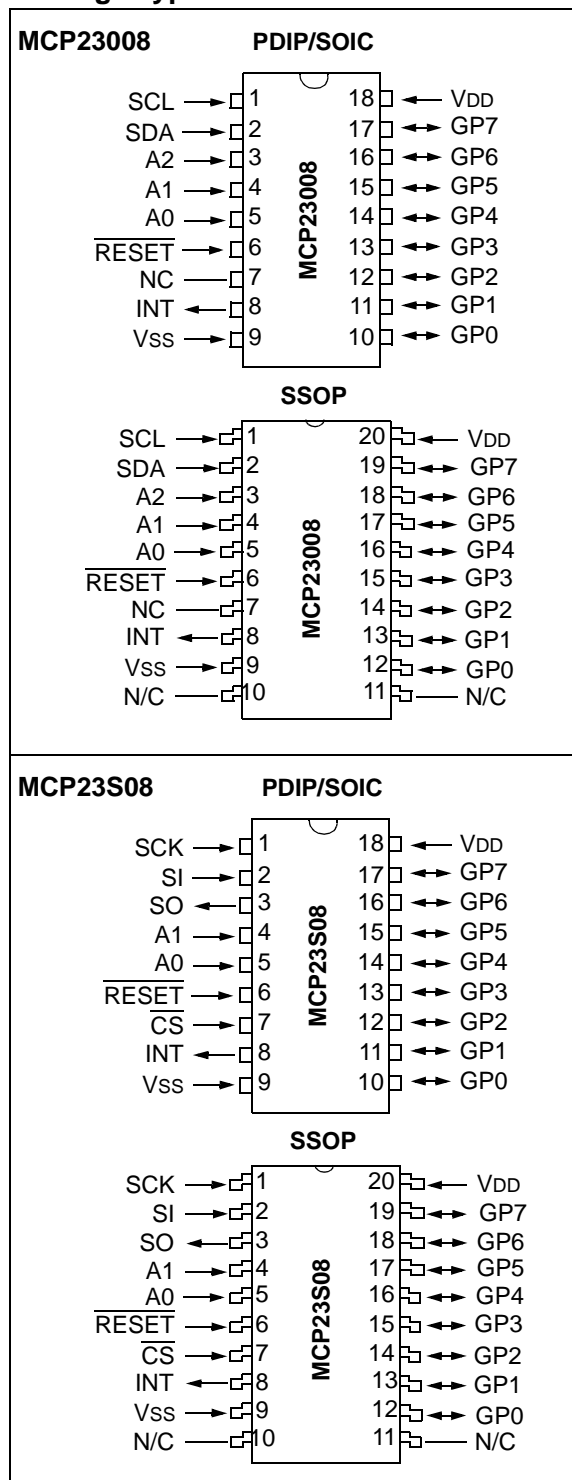
### Packages

18-pin PDIP (300 mil)

18-pin SOIC (300 mil)

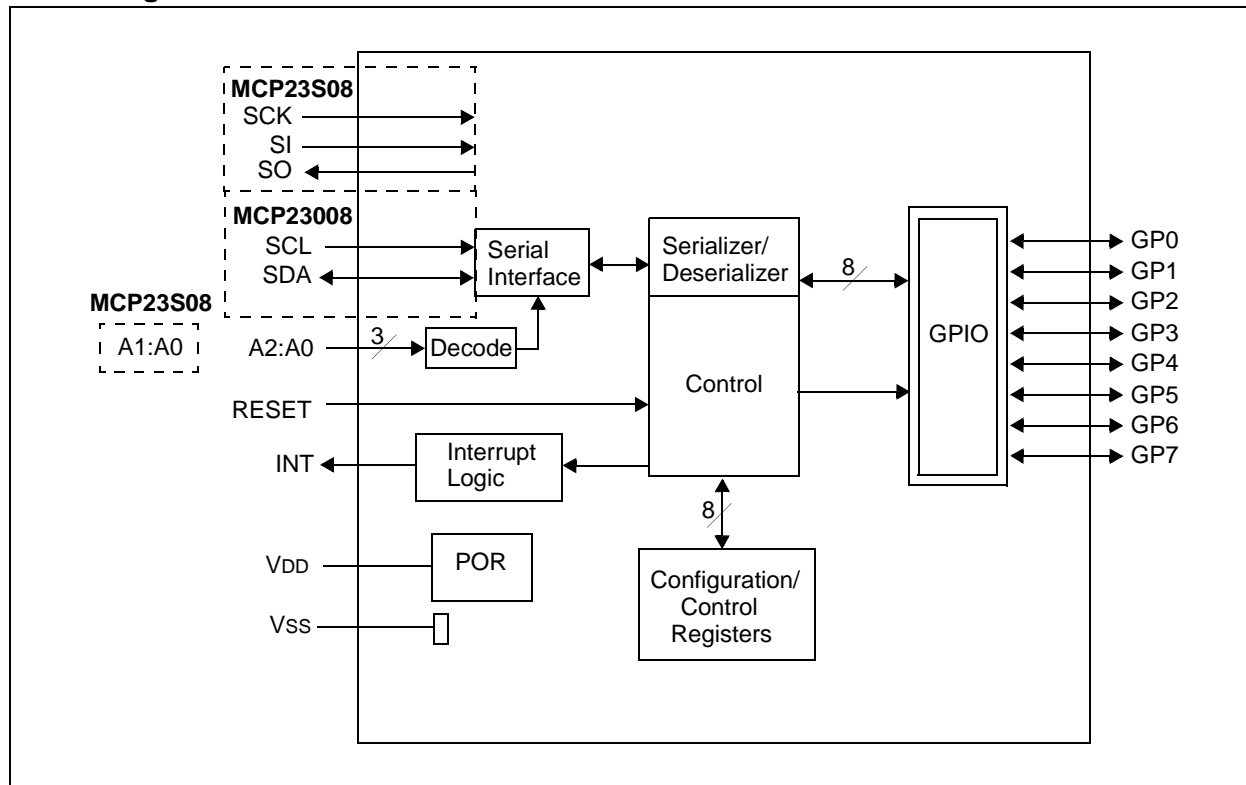
20-pin SSOP

### Package Types



# MCP23008/MCP23S08

## Block Diagram



## 1.0 DEVICE OVERVIEW

The MCP23X08 device provides 8-bit, general purpose parallel I/O expansion for I<sup>2</sup>C bus or SPI applications. The two devices differ in the number of hardware address pins and the serial interface:

- MCP23008 – I<sup>2</sup>C interface; three address pins
- MCP23S08 – SPI interface; two address pins

The MCP23X08 consists of multiple 8-bit configuration registers for input, output and polarity selection. The system master can enable the I/Os as either inputs or outputs by writing the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the input port register can be inverted with the polarity inversion register. All registers can be read by the system master.

The interrupt output can be configured to activate under two conditions (mutually exclusive):

1. When any input state differs from its corresponding input port register state. This is used to indicate to the system master that an input state has changed.
2. When an input state differs from a pre-configured register value (DEFVAL register).

The Interrupt Capture register captures port values at the time of the interrupt, thereby saving the condition that caused the interrupt.

The Power-on Reset (POR) sets the registers to their default values and initializes the device state machine.

The hardware address pins are used to determine the device address.

## 1.1 Pin Descriptions

TABLE 1-1: PINOUT DESCRIPTION

Pin Name	PDIP/ SOIC	SSOP	Pin Type	Function
SCL/SCK	1	1	I	Serial clock input.
SDA/SI	2	2	I/O	Serial data I/O ( <b>MCP23008</b> )/Serial data input ( <b>MCP23S08</b> )
A2/SO	3	3	I/O	Hardware address input ( <b>MCP23008</b> )/Serial data output ( <b>MCP23S08</b> ). A2 must be biased externally.
A1	4	4	I	Hardware address input. Must be biased externally.
A0	5	5	I	Hardware address input. Must be biased externally.
RESET	6	6	I	External reset input
NC/ $\overline{\text{CS}}$	7	7	I	No connect ( <b>MCP23008</b> )/External chip select input ( <b>MCP23S08</b> )
INT	8	8	O	Interrupt output. Can be configured for active-high, active-low or open-drain.
Vss	9	9	P	Ground
GP0	10	12	I/O	Bidirectional I/O Pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP1	11	13	I/O	Bidirectional I/O Pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP2	12	14	I/O	Bidirectional I/O Pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP3	13	15	I/O	Bidirectional I/O Pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP4	14	16	I/O	Bidirectional I/O Pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP5	15	17	I/O	Bidirectional I/O Pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP6	16	18	I/O	Bidirectional I/O Pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP7	17	19	I/O	Bidirectional I/O Pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
VDD	18	20	P	Power
N/C		10, 11		

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## 1.2 Power-on Reset (POR)

The on-chip POR circuit holds the device in reset until VDD has reached a high enough voltage to deactivate the POR circuit (i.e., release the device from reset). The maximum VDD rise time is specified in the electrical specification section.

When the device exits the POR condition (releases reset), device operating parameters (i.e., voltage, temperature, serial bus frequency, etc.) must be met to ensure proper operation.

## 1.3 Serial Interface

This block handles the functionality of the I<sup>2</sup>C (MCP23008) or SPI (MCP23S08) interface protocol. The MCP23X08 contains eleven registers which can be addressed through the Serial Interface block (Table 1-2):

TABLE 1-2: REGISTER ADDRESSES

Address	Access to:
00h	IODIR
01h	IPOL
02h	GPINTEN
03h	DEFVAL
04h	INTCON
05h	IOCON
06h	GPPU
07h	INTF
08h	INTCAP (Read-only)
09h	GPIO
0Ah	OLAT

### 1.3.1 SEQUENTIAL OPERATION BIT

The Sequential Operation (SEQOP) bit (IOCON register) controls the operation of the address pointer. The address pointer can either be enabled (default) to allow the address pointer to increment automatically after each data transfer, or it can be disabled.

When operating in **Sequential mode** (IOCON.SEQOP = 0), the address pointer automatically increments to the next address after each byte is clocked.

When operating in **Byte mode** (IOCON.SEQOP = 1), the MCP23X08 does not increment its address counter after each byte during the data transfer. This gives the ability to continually read the same address by providing extra clocks (without additional control bytes). This is useful for polling the GPIO register for data changes.

### 1.3.2 I<sup>2</sup>C INTERFACE

#### 1.3.2.1 I<sup>2</sup>C Write Operation

The I<sup>2</sup>C write operation includes the control byte and register address sequence, as shown in the bottom of Figure 1-1. This sequence is followed by eight bits of data from the master and an Acknowledge (ACK) from the MCP23008. The operation is ended with a Stop or Restart condition being generated by the master.

Data is written to the MCP23008 after every byte transfer. If a stop or re-start condition is generated during a data transfer, the data will not be written to the MCP23008.

Both byte writes and sequential writes are supported by the MCP23008. The MCP23008 increments its address counter after each ACK during the data transfer.

#### 1.3.2.2 I<sup>2</sup>C Read Operation

I<sup>2</sup>C read operations include the control byte sequence, as shown in the bottom of Figure 1-1. This sequence is followed by another control byte (including the Start condition and ACK) with the R/W bit equal to a logic one (R/W = 1). The MCP23008 then transmits the data contained in the addressed register. The sequence is ended with the master generating a Stop or Restart condition.

#### 1.3.2.3 I<sup>2</sup>C Sequential Write/Read

For sequential operations (Write or Read), instead of transmitting a Stop or Restart condition after the data transfer, the master clocks the next byte pointed to by the address pointer (see **Section 1.3.1 “Sequential Operation Bit”** for details regarding sequential operation control).

The sequence ends with the master sending a Stop or Restart condition.

The MCP23008 address pointer will roll over to address zero after reaching the last register address.

Refer to Figure 1-1.

### 1.3.3 SPI INTERFACE

#### 1.3.3.1 SPI Write Operation

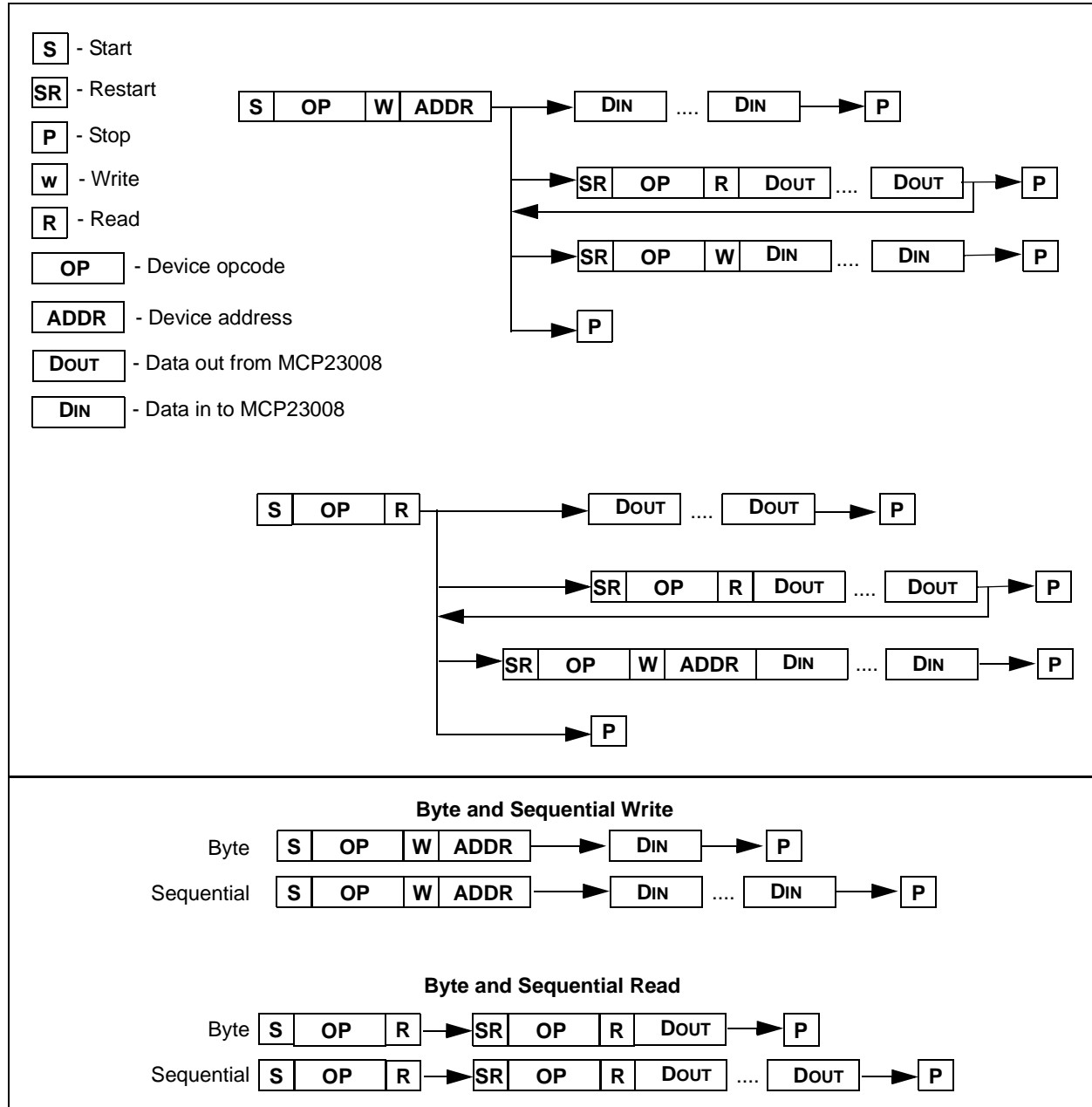
The SPI write operation is started by lowering  $\overline{CS}$ . The Write command (slave address with R/W bit cleared) is then clocked into the device. The opcode is followed by an address and at least one data byte.

#### 1.3.3.2 SPI Read Operation

The SPI read operation is started by lowering  $\overline{CS}$ . The SPI read command (slave address with R/W bit set) is then clocked into the device. The opcode is followed by an address, with at least one data byte being clocked out of the device.

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**FIGURE 1-1: MCP23008 I<sup>2</sup>C™ DEVICE PROTOCOL**



## 1.3.3.3 SPI Sequential Write/Read

For sequential operations, instead of deselecting the device by raising  $\overline{CS}$ , the master clocks the next byte pointed to by the address pointer.

The sequence ends by the raising of  $\overline{CS}$ .

The MCP23S08 address pointer will roll over to address zero after reaching the last register address.

## 1.4 Hardware Address Decoder

The hardware address pins are used to determine the device address. To address a device, the corresponding address bits in the control byte must match the pin state.

- MCP23008 has address pins A2, A1 and A0.
- MCP23S08 has address pins A1 and A0.

The pins must be biased externally.

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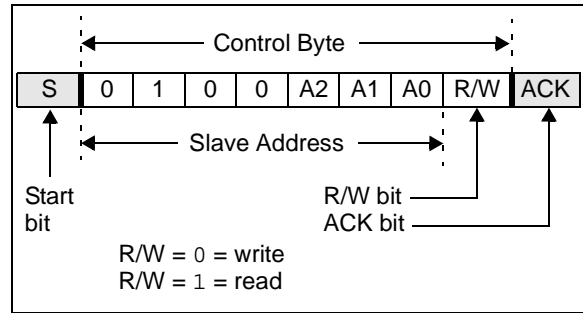
## 1.4.1 ADDRESSING I<sup>2</sup>C DEVICES (MCP23008)

The MCP23008 is a slave I<sup>2</sup>C device that supports 7-bit slave addressing, with the read/write bit filling out the control byte. The slave address contains four fixed bits and three user-defined hardware address bits (pins A2, A1 and A0). Figure 1-2 shows the control byte format.

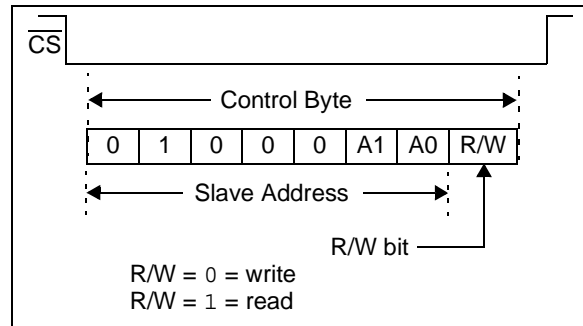
## 1.4.2 ADDRESSING SPI DEVICES (MCP23S08)

The MCP23S08 is a slave SPI device. The slave address contains five fixed bits and two user-defined hardware address bits (pins A1 and A0) with the read/write bit filling out the control byte. Figure 1-3 shows the control byte format.

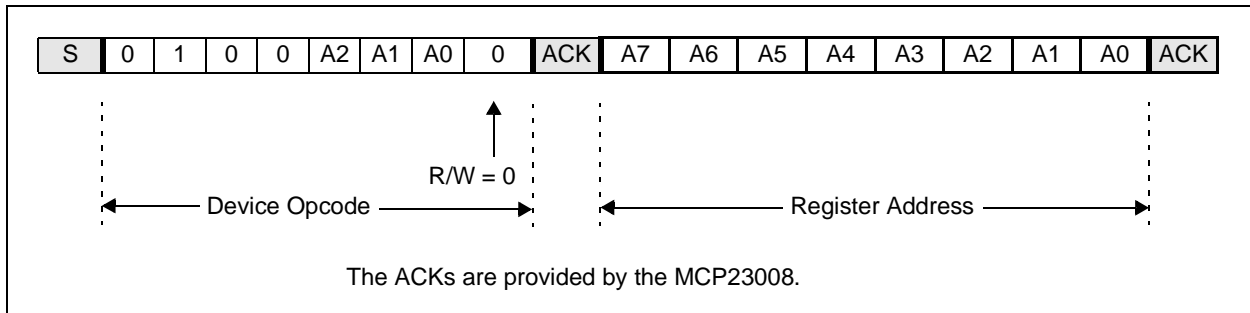
**FIGURE 1-2: I<sup>2</sup>C™ CONTROL BYTE FORMAT**



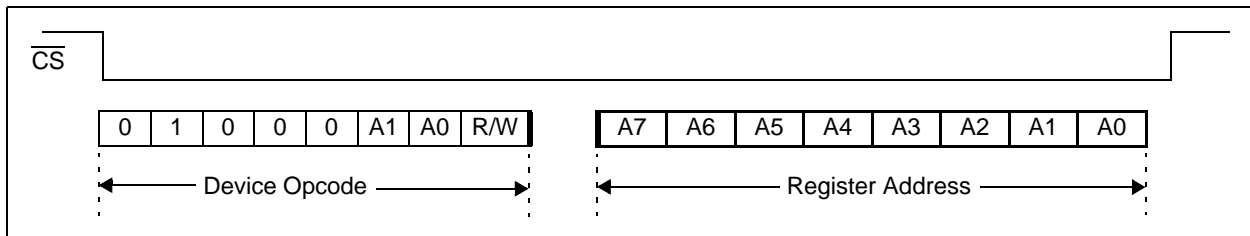
**FIGURE 1-3: SPI™ CONTROL BYTE FORMAT**



**FIGURE 1-4: I<sup>2</sup>C™ ADDRESSING REGISTERS**



**FIGURE 1-5: SPI™ ADDRESSING REGISTERS**



## 1.5 GPIO Port

The GPIO module contains the data port (GPIO), internal pull up resistors and the Output Latches (OLAT).

Reading the GPIO register reads the value on the port. Reading the OLAT register only reads the OLAT, not the actual value on the port.

Writing to the GPIO register actually causes a write to the OLAT. Writing to the OLAT register forces the associated output drivers to drive to the level in OLAT. Pins configured as inputs turn off the associated output driver and put it in high-impedance.

## 1.6 Configuration and Control Registers

The Configuration and Control blocks contain the registers as shown in Table 1-3.

**TABLE 1-3: CONFIGURATION AND CONTROL REGISTERS**

Register Name	Address (hex)	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	POR/RST value
IODIR	00	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IPOL	01	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
GPINTEN	02	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
DEFVAL	03	DEF7	DEF6	DEF5	DEF4	DEF3	DEF2	DEF1	DEF0	0000 0000
INTCON	04	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	0000 0000
IOCON	05	—	—	SREAD	DISSLW	—	ODR	INTPOL	—	--00 -00-
GPPU	06	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000
INTF	07	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0	0000 0000
INTCAP	08	ICP7	ICP6	ICP5	ICP4	ICP3	ICP2	ICP1	ICP0	0000 0000
GPIO	09	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
OLAT	0A	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000

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## 1.6.1 I/O DIRECTION REGISTER

Controls the direction of the data I/O.

When a bit is set, the corresponding pin becomes an input. When a bit is clear, the corresponding pin becomes an output.

### REGISTER 1-1: IODIR – I/O DIRECTION REGISTER (ADDR 0x00)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
bit 7				bit 0			

bit 7-0     **IO7:IO0:** Controls the direction of data I/O <7:0>.

1 = Pin is configured as an input.

0 = Pin is configured as an output.

<b>Legend:</b>		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared     x = Bit is unknown



## 1.6.2 INPUT POLARITY REGISTER

This register allows the user to configure the polarity on the corresponding GPIO port bits.

If a bit is set, the corresponding GPIO register bit will reflect the inverted value on the pin.

### REGISTER 1-2: IPOL – INPUT POLARITY PORT REGISTER (ADDR 0x01)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
bit 7				bit 0			

bit 7-0 **IP7:IP0:** Controls the polarity inversion of the input pins <7:0>.  
1 = GPIO register bit will reflect the opposite logic state of the input pin.  
0 = GPIO register bit will reflect the same logic state of the input pin.

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared    x = Bit is unknown

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## 1.6.3 INTERRUPT-ON-CHANGE CONTROL REGISTER

The GPINTEN register controls the interrupt-on-change feature for each pin.

If a bit is set, the corresponding pin is enabled for interrupt-on-change. The DEFVAL and INTCON registers must also be configured if any pins are enabled for interrupt-on-change.

### REGISTER 1-3: GPINTEN – INTERRUPT-ON-CHANGE PINS (ADDR 0x02)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0
bit 7							bit 0

bit 7-0      **GPINT7:GPINT0:** General purpose I/O interrupt-on-change pins <7:0>.  
1 = Enable GPIO input pin for interrupt-on-change event.  
0 = Disable GPIO input pin for interrupt-on-change event.

Refer to INTCON and GPINTEN.

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

## 1.6.4 DEFAULT COMPARE REGISTER FOR INTERRUPT-ON-CHANGE

The default comparison value is configured in the DEFVAL register. If enabled (via GPINTEN and INTCON) to compare against the DEFVAL register, an opposite value on the associated pin will cause an interrupt to occur.

### REGISTER 1-4: DEFVAL – DEFAULT VALUE REGISTER (ADDR 0x03)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DEF7	DEF6	DEF5	DEF4	DEF3	DEF2	DEF1	DEF0
bit 7				bit 0			

bit 7-0 **DEF7:DEF0:** Sets the compare value for pins configured for interrupt-on-change from defaults <7:0>. Refer to INTCON.

If the associated pin level is the opposite from the register bit, an interrupt occurs.

Refer to INTCON and GPINTEN.

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared    x = Bit is unknown

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## 1.6.5 INTERRUPT CONTROL REGISTER

The INTCON register controls how the associated pin value is compared for the interrupt-on-change feature. If a bit is set, the corresponding I/O pin is compared against the associated bit in the DEFVAL register. If a bit value is clear, the corresponding I/O pin is compared against the previous value.

### REGISTER 1-5: INTCON – INTERRUPT-ON-CHANGE CONTROL REGISTER (ADDR 0x04)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0
bit 7				bit 0			

bit 7-0     **IOC7:IOC0:** Controls how the associated pin value is compared for interrupt-on-change <7:0>.

- 1 = Controls how the associated pin value is compared for interrupt-on-change.
- 0 = Pin value is compared against the previous pin value.

Refer to INTCON and GPINTEN.

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

## 1.6.6 CONFIGURATION REGISTER

The IOCON register contains several bits for configuring the device:

- The Sequential Operation (SEQOP) controls the incrementing function of the address pointer. If the address pointer is disabled, the address pointer does not automatically increment after each byte is clocked during a serial transfer. This feature is useful when it is desired to continuously poll (read) or modify (write) a register.
- The slew rate (DISSLW) bit controls the slew rate function on the SDA pin. If enabled, the SDA slew rate will be controlled when driving from a high to low.
- The Open-Drain (ODR) control bit enables/disables the INT pin for open-drain configuration.
- The Interrupt Polarity (INTPOL) sets the polarity of the INT pin. This bit is functional only when the ODR bit is cleared, configuring the INT pin as active push-pull.

### REGISTER 1-6: IOCON – I/O EXPANDER CONFIGURATION REGISTER (ADDR 0x05)

U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
—	—	SEQOP	DISSLW	—	ODR	INTPOL	—
bit 7				bit 0			

bit 7-6 **Unimplemented:** Read as '0'.

bit 5 **SEQOP:** Sequential Operation mode bit.

- 1 = Sequential operation disabled, address pointer does not increment.
- 0 = Sequential operation enabled, address pointer increments.

bit 4 **DISSLW:** Slew rate control for SDA output.

- 1 = Slew rate disabled.
- 0 = Slew rate enabled.

bit 3 **Unimplemented:** Read as '0'.

bit 2 **ODR:** Configures the INT pin as an open-drain output.

- 1 = Open-drain output (overrides the INTPOL bit).
- 0 = Active driver output (INTPOL bit sets the polarity).

bit 1 **INTPOL:** Sets the polarity of the INT output pin.

- 1 = Active-high.
- 0 = Active-low.

bit 0 **Unimplemented:** Read as '0'.

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared    x = Bit is unknown

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## 1.6.7 PULL-UP RESISTOR CONFIGURATION REGISTER

The GPPU register controls the pull-up resistors for the port pins. If a bit is set and the corresponding pin is configured as an input, the corresponding port pin is internally pulled up with a 100 kΩ resistor.

### REGISTER 1-7: GPPU – GPIO PULL-UP RESISTOR REGISTER (ADDR 0x06)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0
bit 7				bit 0			

bit 7-0     **PU7:PU0:** Controls the weak pull-up resistors on each pin (when configured as an input) <7:0>.

1 = Pull-up enabled.  
0 = Pull-up disabled.

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

## 1.6.8 INTERRUPT FLAG REGISTER

The INTF register reflects the interrupt condition on the port pins of any pin that is enabled for interrupts via the GPINTEN register. A 'set' bit indicates that the associated pin caused the interrupt.

This register is 'read only'. Writes to this register will be ignored.

### REGISTER 1-8: INTF – INTERRUPT FLAG REGISTER (ADDR 0x07)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
bit 7				bit 0			

bit 7-0 **INT7:INT0:** Reflects the interrupt condition on the port. Will reflect the change only if interrupts are enabled (GPINTEN) <7:0>.

1 = Pin caused interrupt.

0 = Interrupt not pending.

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

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## 1.6.9 INTERRUPT CAPTURE REGISTER

The INTCAP register captures the GPIO port value at the time the interrupt occurred. The register is 'read only' and is updated only when an interrupt occurs. The register will remain unchanged until the interrupt is cleared via a read of INTCAP or GPIO.

### REGISTER 1-9: INTCAP – INTERRUPT CAPTURED VALUE FOR PORT REGISTER (ADDR 0x08)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ICP7	ICP6	ICP5	ICP4	ICP3	ICP2	ICP1	ICP0
bit 7				bit 0			

bit 7-0      **ICP7:ICP0:** Reflects the logic level on the port pins at the time of interrupt due to pin change <7:0>.  
1 = Logic-high.  
0 = Logic-low.

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown



## 1.6.10 PORT REGISTER

The GPIO register reflects the value on the port.  
Reading from this register reads the port. Writing to this register modifies the Output Latch (OLAT) register.

### REGISTER 1-10: GPIO – GENERAL PURPOSE I/O PORT REGISTER (ADDR 0x09)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0
bit 7				bit 0			

bit 7-0     **GP7:GP0:** Reflects the logic level on the pins <7:0>.  
1 = Logic-high.  
0 = Logic-low.

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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## 1.6.11 OUTPUT LATCH REGISTER (OLAT)

The OLAT register provides access to the output latches. A read from this register results in a read of the OLAT and not the port itself. A write to this register modifies the output latches that modifies the pins configured as outputs.

### REGISTER 1-11: OLAT – OUTPUT LATCH REGISTER 0 (ADDR 0x0A)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0
bit 7				bit 0			

bit 7-0      **OL7:OL0:** Reflects the logic level on the output latch <7:0>.  
1 = Logic-high.  
0 = Logic-low.

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

## 1.7 Interrupt Logic

The interrupt output pin will activate if an internal interrupt occurs. The interrupt block is configured by the following registers:

- GPINTEN – enables the individual inputs
- DEFVAL – holds the values that are compared against the associated input port values
- INTCON – controls if the input values are compared against DEFVAL or the previous values on the port
- IOCON (ODR and INPOL) – configures the INT pin as push-pull, open-drain and active-level

Only pins configured as inputs can cause interrupts. Pins configured as outputs have no effect on INT.

Interrupt activity on the port will cause the port value to be captured and copied into INTCAP. The interrupt will remain active until the INTCAP or GPIO register is read. Writing to these registers will not affect the interrupt.

The first interrupt event will cause the port contents to be copied into the INTCAP register. Subsequent interrupt conditions on the port will not cause an interrupt to occur as long as the interrupt is not cleared by a read of INTCAP or GPIO.

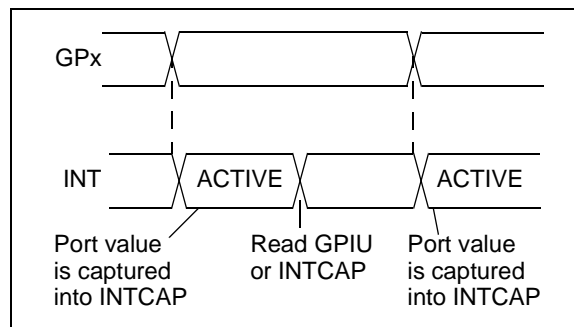
### 1.7.1 INTERRUPT CONDITIONS

There are two possible configurations to cause interrupts (configured via INTCON):

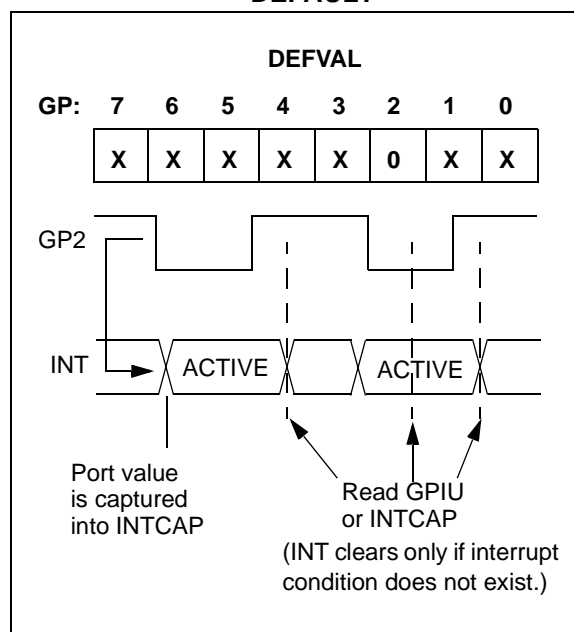
1. Pins configured for **interrupt-on-pin-change** will cause an interrupt to occur if a pin changes to the opposite state. The default state is reset after an interrupt occurs. For example, an interrupt occurs by an input changing from 1 to 0. The new initial state for the pin is a logic 0.
2. Pins configured for **interrupt-on-change from register value** will cause an interrupt to occur if the corresponding input pin differs from the register bit. The interrupt condition will remain as long as the condition exists, regardless if the INTAP or GPIO is read.

See Figure 1-6 and Figure 1-7 for more information on interrupt operations.

**FIGURE 1-6: INTERRUPT-ON-PIN-CHANGE**



**FIGURE 1-7: INTERRUPT-ON-CHANGE FROM REGISTER DEFAULT**



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NOTES:

## 2.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Ambient temperature under bias .....	-40°C to +125°C
Storage temperature .....	-65°C to +150°C
Voltage on VDD with respect to VSS .....	-0.3V to +5.5V
Voltage on all other pins with respect to VSS (except VDD).....	-0.6V to (VDD + 0.6V)
Total power dissipation ( <b>Note</b> ) .....	700 mW
Maximum current out of VSS pin .....	150 mA
Maximum current into VDD pin .....	125 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > VDD).....	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > VDD) .....	±20 mA
Maximum output current sunk by any output pin .....	25 mA
Maximum output current sourced by any output pin .....	25 mA

**Note:** Power dissipation is calculated as follows:

$$P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$$

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

# MCP23008/MCP23S08

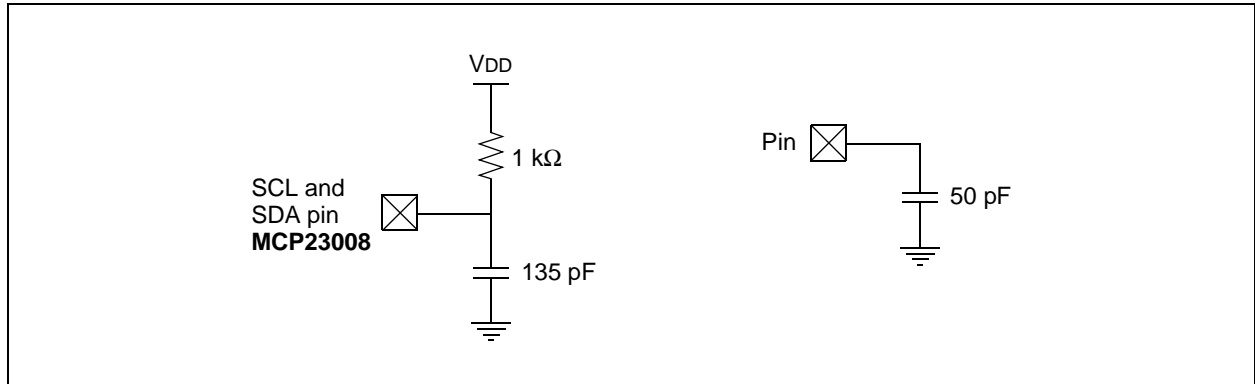
## 2.1 DC Characteristics

DC Characteristics		Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) (Note 1)					
Param No.	Characteristic	Sym	Min	Typ	Max	Units	Conditions
D001	Supply Voltage	VDD	1.8	—	5.5	V	
D002	VDD Start Voltage to Ensure Power-on Reset	VPOR	—	VSS	—	V	
D003	VDD Rise Rate to Ensure Power-on Reset	SVDD	0.05	—	—	V/ms	Design guidance only. Not tested.
D004	Supply Current	IDD	—	—	1	mA	SCL/SCK = 1 MHz
D005	Standby current	IDDS	—	—	1	μA	
			—	—	2	μA	4.5V - 5.5V @ +125°C (Note 1)
Input Low-Voltage							
D030	A0, A1 (TTL buffer)	VIL	VSS	—	0.15 VDD	V	
D031	CS, GPIO, SCL/SCK, SDA, A2, RESET (Schmitt Trigger)		VSS	—	0.2 VDD	V	
Input High-Voltage							
D040	A0, A1 (TTL buffer)	VIH	0.25 VDD + 0.8	—	VDD	V	
D041	CS, GPIO, SCL/SCK, SDA, A2, RESET (Schmitt Trigger)		0.8 VDD	—	VDD	V	For entire VDD range
Input Leakage Current							
D060	I/O port pins	IIL	—	—	±1	μA	VSS ≤ VPIN ≤ VDD,
Output Leakage Current							
D065	I/O port pins	ILO	—	—	±1	μA	VSS ≤ VPIN ≤ VDD,
D070	GPIO weak pull-up current	IPU	40	75	115	μA	VDD = 5V, GP Pins = VSS -40°C ≤ TA ≤ +85°C
Output Low-Voltage							
D080	GPIO	VOL	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V
	INT		—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V
	SO, SDA		—	—	0.6	V	IOL = 3.0 mA, VDD = 1.8V
	SDA		—	—	0.8	V	IOL = 3.0 mA, VDD = 4.5V
Output High-Voltage							
D090	GPIO, INT, SO	VOH	VDD - 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V
			VDD - 0.7	—	—		IOH = -400 μA, VDD = 1.8V
Capacitive Loading Specs on Output Pins							
D101	GPIO, SO, INT	CIO	—	—	50	pF	
D102	SDA	CB	—	—	400	pF	

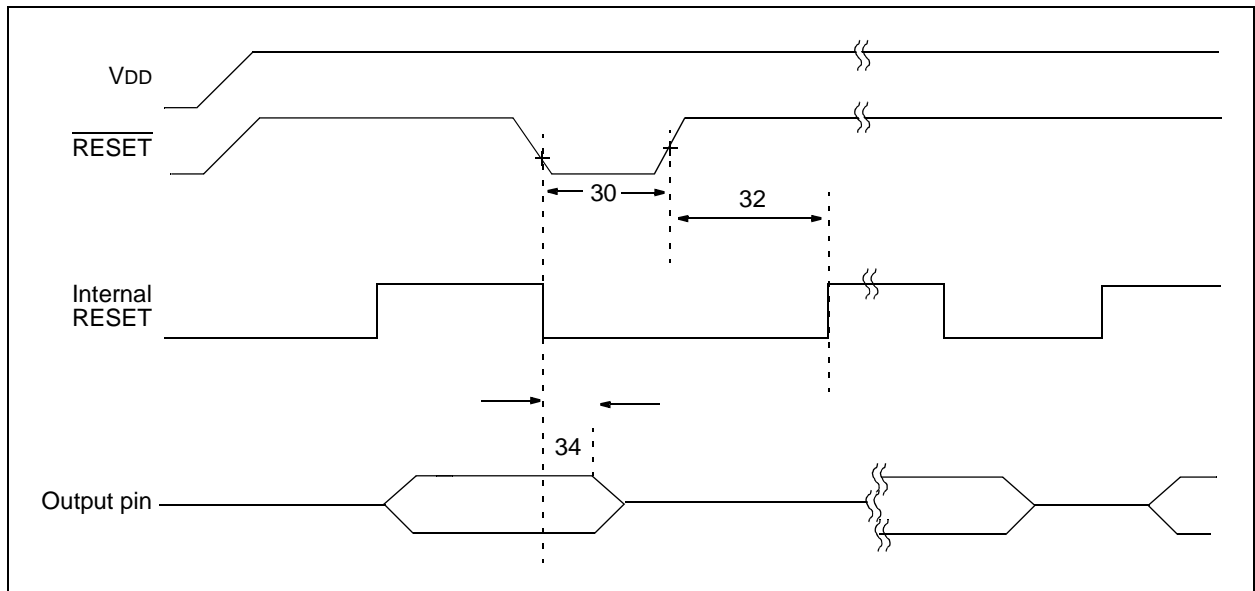
**Note 1:** This parameter is characterized, not 100% tested.

# MCP23008/MCP23S08

**FIGURE 2-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**



**FIGURE 2-2: RESET AND DEVICE RESET TIMER TIMING**



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TABLE 2-1:     DEVICE RESET SPECIFICATIONS

AC Characteristics		Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) (Note 1)					
Param No.	Characteristic	Sym	Min	Typ <sup>(1)</sup>	Max	Units	Conditions
30	RESET Pulse Width (Low)	TRSTL	1	—	—	μs	
32	Device Active After Reset high	THLD	—		TBD	μs	VDD = 5.0V
34	Output High-Impedance From RESET Low	TIOZ	—	—	1	μs	

Note 1: This parameter is characterized, not 100% tested.

FIGURE 2-3:     I<sup>2</sup>C™ BUS START/STOP BITS TIMING

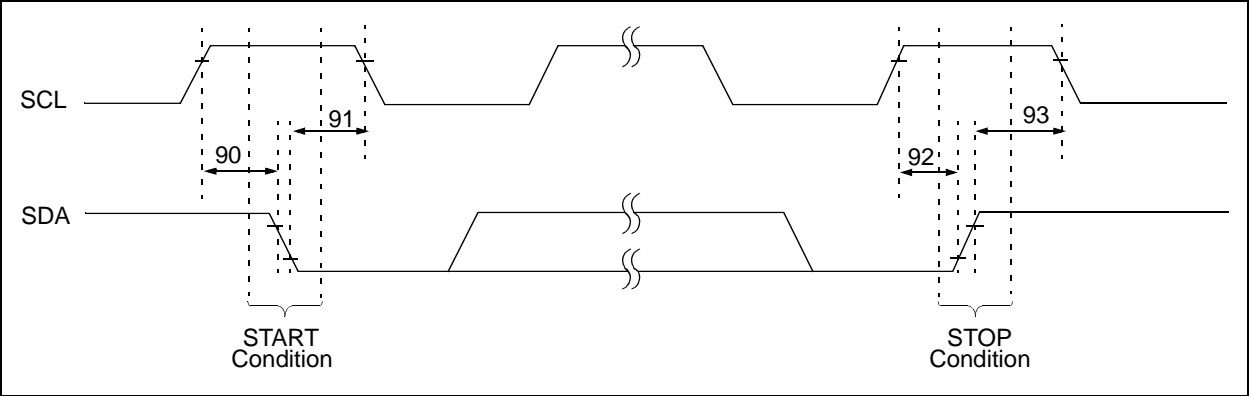
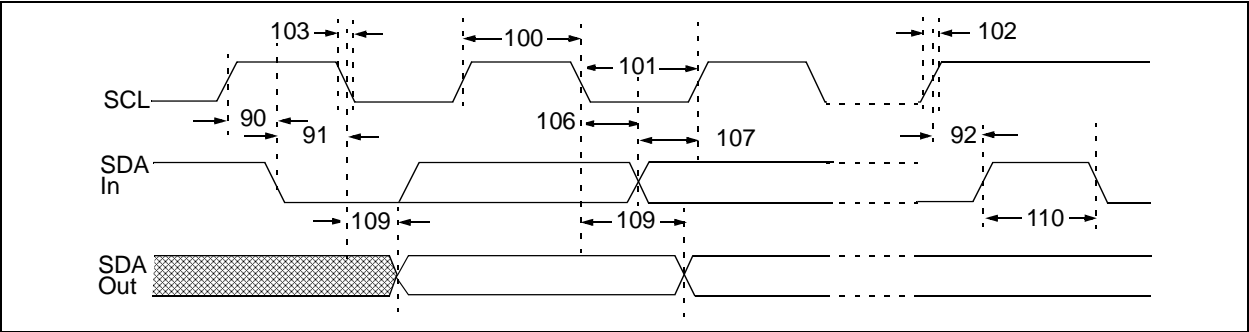


FIGURE 2-4:     I<sup>2</sup>C™ BUS DATA TIMING





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**TABLE 2-2: I<sup>2</sup>C™ BUS DATA REQUIREMENTS (SLAVE MODE)**

I <sup>2</sup> C™ AC Characteristics		Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) (Note 1) RPU (SCL, SDA) = 1 kΩ, CL (SCL, SDA) = 135 pF.					
Param No.	Characteristic	Sym	Min	Typ	Max	Units	Conditions
100	Clock High Time:	THIGH					
	100 kHz mode		4.0	—	—	μs	1.8V – 5.5V (I-Temp)
	400 kHz mode		0.6	—	—	μs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0.12	—	—	μs	4.5V – 5.5V (E-Temp)
101	Clock Low Time:	TLOW					
	100 kHz mode		4.7	—	—	μs	1.8V – 5.5V (I-Temp)
	400 kHz mode		1.3	—	—	μs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0.32	—	—	μs	4.5V – 5.5V (E-Temp)
102	SDA and SCL Rise Time:	TR (Note 1)					
	100 kHz mode		—	—	1000	ns	1.8V – 5.5V (I-Temp)
	400 kHz mode		20 + 0.1 CB <sup>(2)</sup>	—	300	ns	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		20	—	160	ns	4.5V – 5.5V (E-Temp)
103	SDA and SCL Fall Time:	TF (Note 1)					
	100 kHz mode		—	—	300	ns	1.8V – 5.5V (I-Temp)
	400 kHz mode		20 + 0.1 CB <sup>(2)</sup>	—	300	ns	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		20	—	80	ns	4.5V – 5.5V (E-Temp)
90	START Condition Setup Time:	TSU:STA					
	100 kHz mode		4.7	—	—	μs	1.8V – 5.5V (I-Temp)
	400 kHz mode		0.6	—	—	μs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0.16	—	—	μs	4.5V – 5.5V (E-Temp)
91	START Condition Hold Time:	THD:STA					
	100 kHz mode		4.0	—	—	μs	1.8V – 5.5V (I-Temp)
	400 kHz mode		0.6	—	—	μs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0.16	—	—	μs	4.5V – 5.5V (E-Temp)
106	Data Input Hold Time:	THD:DAT					
	100 kHz mode		0	—	3.45	μs	1.8V – 5.5V (I-Temp)
	400 kHz mode		0	—	0.9	μs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0	—	0.15	μs	4.5V – 5.5V (E-Temp)
107	Data Input Setup Time:	TSU:DAT					
	100 kHz mode		250	—	—	ns	1.8V – 5.5V (I-Temp)
	400 kHz mode		100	—	—	ns	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0.01	—	—	μs	4.5V – 5.5V (E-Temp)
92	STOP Condition Setup Time:	TSU:STO					
	100 kHz mode		4.0	—	—	μs	1.8V – 5.5V (I-Temp)
	400 kHz mode		0.6	—	—	μs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0.16	—	—	μs	4.5V – 5.5V (E-Temp)

**Note 1:** This parameter is characterized, not 100% tested.

**Note 2:** CB is specified to be from 10 to 400 pF.

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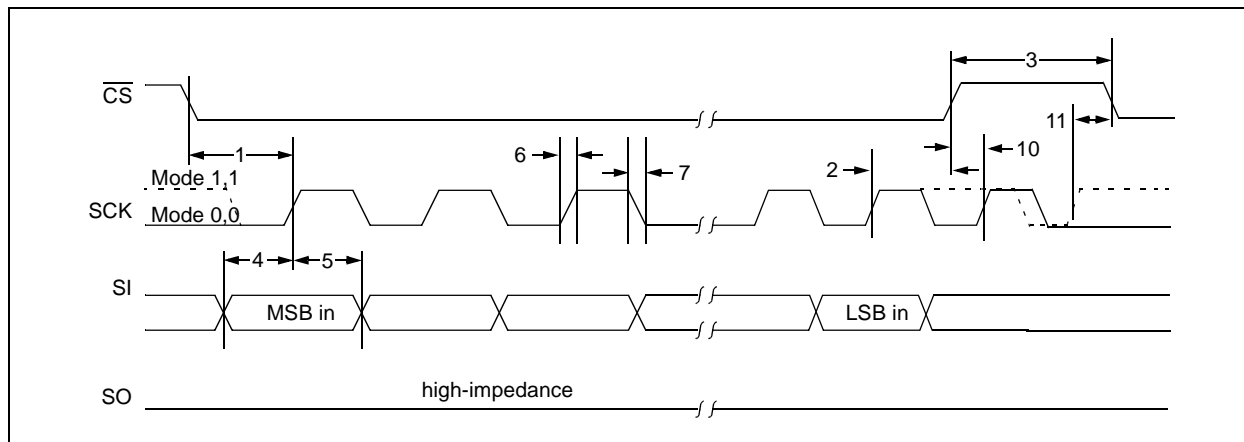
**TABLE 2-2: I<sup>2</sup>C™ BUS DATA REQUIREMENTS (SLAVE MODE) (CONTINUED)**

I <sup>2</sup> C™ AC Characteristics		Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) (Note 1) RPU (SCL, SDA) = 1 kΩ, CL (SCL, SDA) = 135 pF.					
Param No.	Characteristic	Sym	Min	Typ	Max	Units	Conditions
109	Output Valid From Clock:	TAA					
	100 kHz mode		—	—	3.45	μs	1.8V – 5.5V (I-Temp)
	400 kHz mode		—	—	0.9	μs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		—	—	0.18	μs	4.5V – 5.5V (E-Temp)
110	Bus Free Time:	TBUF					
	100 kHz mode		4.7	—	—	μs	1.8V – 5.5V (I-Temp)
	400 kHz mode		1.3	—	—	μs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		N/A	—	N/A	μs	4.5V – 5.5V (E-Temp)
	Bus Capacitive Loading:	CB					
	100 kHz and 400 kHz		—	—	400	pF	(Note 1)
	1.7 MHz		—	—	100	pF	(Note 1)
	Input Filter Spike Suppression: (SDA and SCL)	TSP					
	100 kHz and 400 kHz		—	—	50	ns	
	1.7 MHz		—	—	10	ns	Spike suppression off

**Note 1:** This parameter is characterized, not 100% tested.

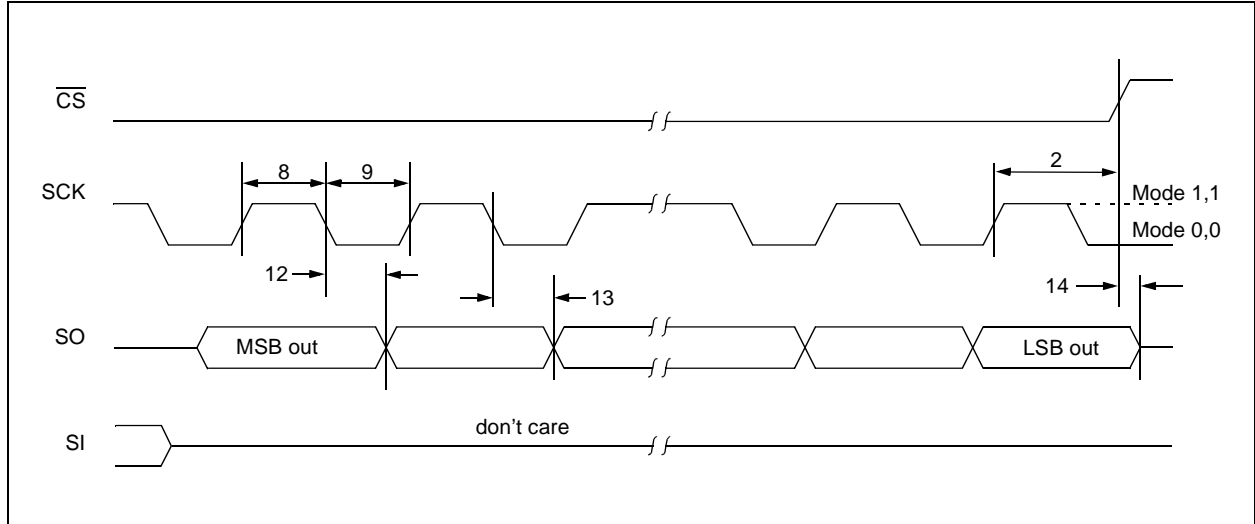
**2:** CB is specified to be from 10 to 400 pF.

**FIGURE 2-5: SPI™ INPUT TIMING**



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**FIGURE 2-6: SPI™ OUTPUT TIMING**



**TABLE 2-3: SPI™ INTERFACE AC CHARACTERISTICS**

SPI™ Interface AC Characteristics		Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) (Note 1)					
Param No.	Characteristic	Sym	Min	Typ	Max	Units	Conditions
	Clock Frequency	FCLK	—	—	5	MHz	1.8V – 5.5V (I-Temp)
			—	—	10	MHz	2.7V – 5.5V (I-Temp)
			—	—	10	MHz	4.5V – 5.5V (E-Temp)
1	$\overline{CS}$ Setup Time	T <sub>CSS</sub>	50	—	—	ns	
2	$\overline{CS}$ Hold Time	T <sub>CSH</sub>	100	—	—	ns	1.8V – 5.5V (I-Temp)
			50	—	—	ns	2.7V – 5.5V (I-Temp)
			50	—	—	ns	4.5V – 5.5V (E-Temp)
3	$\overline{CS}$ Disable Time	T <sub>CSD</sub>	100	—	—	ns	1.8V – 5.5V (I-Temp)
			50	—	—	ns	2.7V – 5.5V (I-Temp)
			50	—	—	ns	4.5V – 5.5V (E-Temp)
4	Data Setup Time	T <sub>SU</sub>	20	—	—	ns	1.8V – 5.5V (I-Temp)
			10	—	—	ns	2.7V – 5.5V (I-Temp)
			10	—	—	ns	4.5V – 5.5V (E-Temp)
5	Data Hold Time	T <sub>HD</sub>	20	—	—	ns	1.8V – 5.5V (I-Temp)
			10	—	—	ns	2.7V – 5.5V (I-Temp)
			10	—	—	ns	4.5V – 5.5V (E-Temp)
6	CLK Rise Time	T <sub>R</sub>	—	—	2	μs	Note 1
7	CLK Fall Time	T <sub>F</sub>	—	—	2	μs	Note 1
8	Clock High Time	T <sub>HI</sub>	90	—	—	ns	1.8V – 5.5V (I-Temp)
			45	—	—	ns	2.7V – 5.5V (I-Temp)
			45	—	—	ns	4.5V – 5.5V (E-Temp)

**Note 1:** This parameter is characterized, not 100% tested.

**2:** T<sub>v</sub> = 90 ns (max) when address pointer rolls over from address 0x0A to 0x00.

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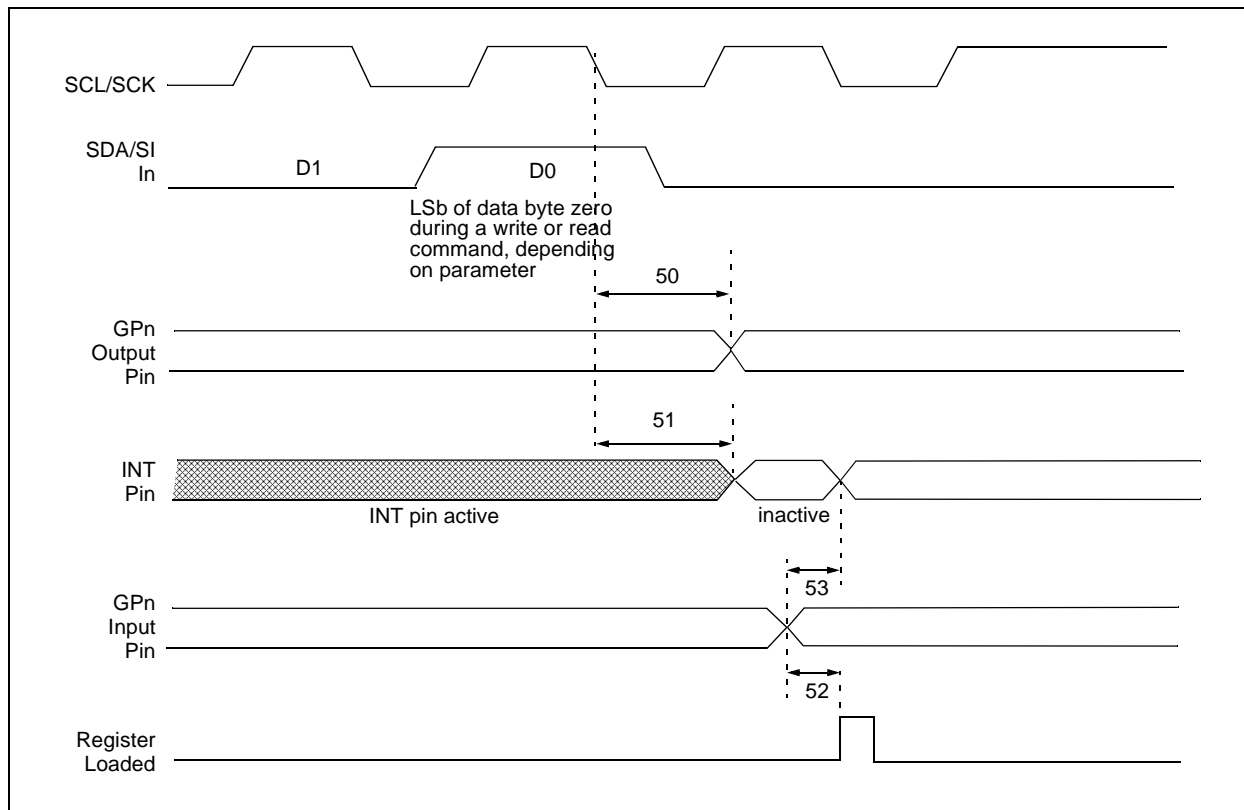
**TABLE 2-3: SPI™ INTERFACE AC CHARACTERISTICS (CONTINUED)**

SPI™ Interface AC Characteristics		Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) (Note 1)					
Param No.	Characteristic	Sym	Min	Typ	Max	Units	Conditions
9	Clock Low Time	TLO	90	—	—	ns	1.8V – 5.5V (I-Temp)
			45	—	—	ns	2.7V – 5.5V (I-Temp)
			45	—	—	ns	4.5V – 5.5V (E-Temp)
10	Clock Delay Time	TCLD	50	—	—	ns	
11	Clock Enable Time	TCLE	50	—	—	ns	
12	Output Valid from Clock Low	TV	—	—	90	ns	1.8V – 5.5V (I-Temp)
			—	—	45	ns	2.7V – 5.5V (I-Temp)
			—	—	45	ns	4.5V – 5.5V (E-Temp)
13	Output Hold Time	THO	0	—	—	ns	
14	Output Disable Time	TDIS	—	—	100	ns	

**Note 1:** This parameter is characterized, not 100% tested.

**2:** Tv = 90 ns (max) when address pointer rolls over from address 0x0A to 0x00.

**FIGURE 2-7: GPIO AND INT TIMING**



**TABLE 2-4: GP AND INT PINS**

AC Characteristics		Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) (Note 1)					
Param No.	Characteristic	Sym	Min	Typ	Max	Units	Conditions
50	Serial data to output valid	TGPOV	—	—	500	ns	
51	Interrupt pin disable time	TINTD	—	—	450	ns	
52	GP input change to register valid	TGPIV	—	—	450	ns	
53	IOC event to INT active	TGPINT	—	—	500	ns	
	Glitch Filter on GP Pins	TGLITCH	—	—	150	ns	

**Note 1:** This parameter is characterized, not 100% tested

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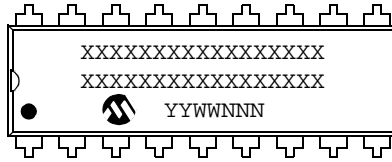
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NOTES:

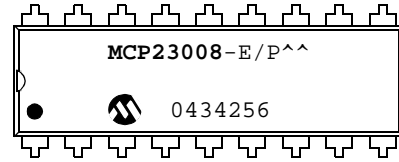
## 3.0 PACKAGING INFORMATION

### 3.1 Package Marking Information

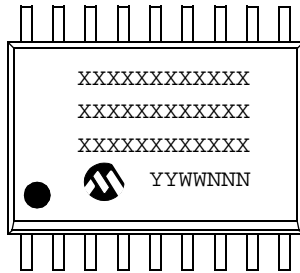
18-Lead PDIP (300 mil)



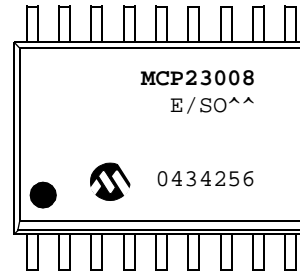
Example:



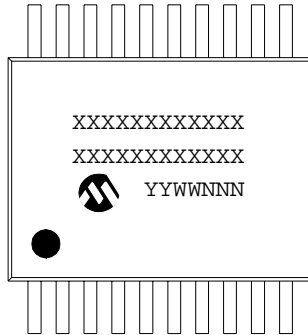
18-Lead SOIC (300 mil)



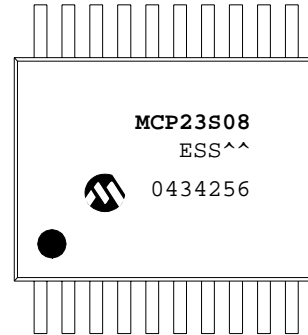
Example:



20-Lead SSOP



Example:



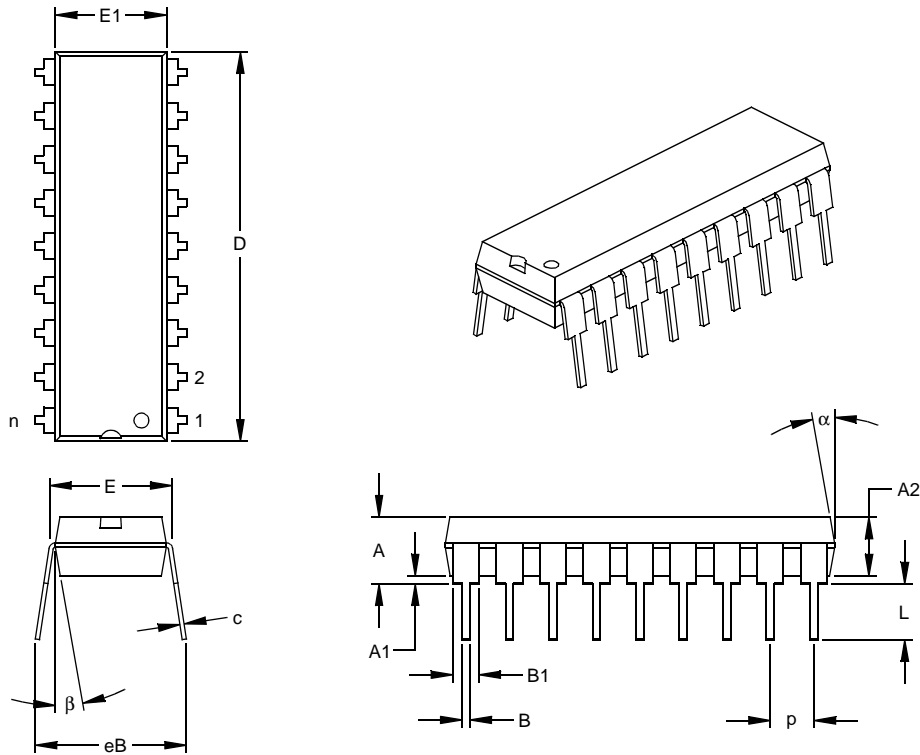
<b>Legend:</b>	XX...X	Customer specific information*
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	"^^"	Indicates Pb-free packaging

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

\* Standard device marking consists of Microchip part number, year code, week code, and traceability code.

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## 18-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.890	.898	.905	22.61	22.80	22.99
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

\* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

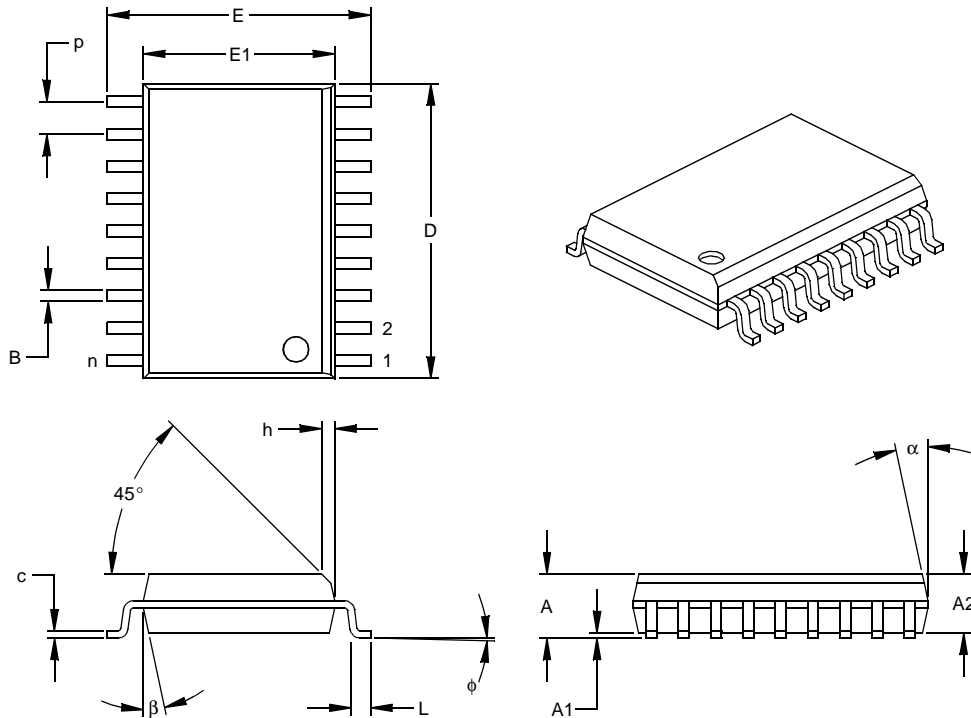
JEDEC Equivalent: MS-001

Drawing No. C04-007



# MCP23008/MCP23S08

## 18-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.012	0.23	0.27	0.30
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter

§ Significant Characteristic

### Notes:

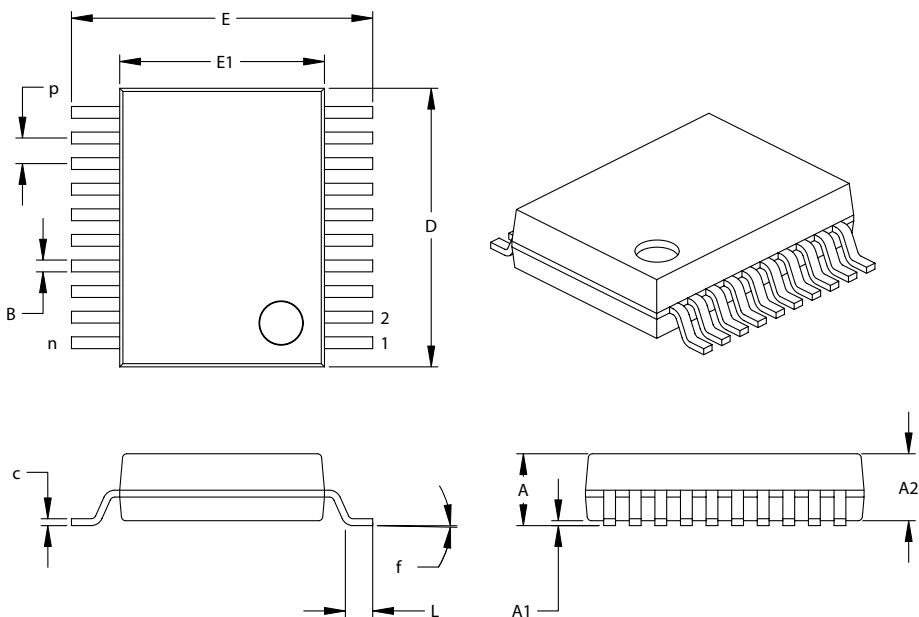
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-013

Drawing No. C04-051

# MCP23008/MCP23S08

20-Lead Plastic Shrink Small Outline (SS) – 209 mil Body, 5.30 mm (SSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	20			20		
Pitch	P		.026			0.65	
Overall Height	A	-	-	.079	-	-	2.00
Molded Package Thickness	A2	.065	.069	.073	1.65	1.75	1.85
Standoff	A1	.002	-	-	0.05	-	-
Overall Width	E	.291	.307	.323	7.40	7.80	8.20
Molded Package Width	E1	.197	.209	.220	5.00	5.30	5.60
Overall Length	D	.272	.283	.289	.295	7.20	7.50
Foot Length	L	.022	.030	.037	0.55	0.75	0.95
Lead Thickness	c	.004	-	.010	0.09	-	0.25
Foot Angle	f	0°	4°	8°	0°	4°	8°
Lead Width	B	.009	-	.015	0.22	-	0.38

\*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-150  
Drawing No. C04-072

Revised 11/03/03

## APPENDIX A: REVISION HISTORY

### Revision A (December 2004)

Original data sheet release.

# MCP23008/MCP23S08

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NOTES:

# MCP23008/MCP23S08

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	-	<u>X</u>	<u>/XX</u>
Device		Temperature Range	Package
Device	MCP23008:	8-Bit I/O Expander w/ I <sup>2</sup> C™ Interface	
	MCP23008T:	8-Bit I/O Expander w/ I <sup>2</sup> C Interface (Tape and Reel)	
	MCP23S08:	8-Bit I/O Expander w/ SPI™ Interface	
	MCP23S08T:	8-Bit I/O Expander w/ SPI Interface (Tape and Reel)	
Temperature Range	E	= -40°C to +125°C (Extended) *	
		* While these devices are only offered in the “E” temperature range, the device will operate at different voltages and temperatures as identified in the <b>Section 2.0, “Electrical Characteristics”</b> .	
Package	P	= Plastic DIP (300 mil Body), 18-Lead	
	SO	= Plastic SOIC (300 mil Body), 18-Lead	
	SS	= SSOP, (209 mil Body, 5.30 mm), 20-Lead	

**Examples:**  
a) MCP23008-E/P: Extended Temp., 18LD PDIP package.  
b) MCP23008-E/SO: Extended Temp., 18LD SOIC package.  
c) MCP23008T-E/SO: Tape and Reel, Extended Temp., 18LD SOIC package.  
d) MCP23008-E/SS: Extended Temp., 20LD SSOP package.  
e) MCP23008T-E/SS: Tape and Reel, Extended Temp., 20LD SSOP package.  
  
a) MCP23S08-E/P: Extended Temp., 18LD PDIP package.  
b) MCP23S08-E/SO: Extended Temp., 18LD SOIC package.  
c) MCP23S08T-E/SO: Tape and Reel, Extended Temp., 18LD SOIC package.  
d) MCP23S08-E/SS: Extended Temp., 20LD SSOP package.  
e) MCP23S08T-E/SS: Tape and Reel, Extended Temp., 20LD SSOP package.

## Sales and Support

### Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Worldwide Site ([www.microchip.com](http://www.microchip.com))

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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# MCP23008/MCP23S08

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NOTES:

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**Note the following details of the code protection feature on Microchip devices:**

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