GENERAL DESCRIPTION

The XRP6272 is a low dropout voltage regulator capable of a constant output current up to 2 Amps. A wide 1.8V to 6V input voltage range allows for single supply operations from industry standard 1.8V, 2.8V, 3.3V, and 5V power rails as well as the 5.8V rail.

With better than ±2% output voltage accuracy, low output noise and high Power Supply Rejection Ratio (PSRR), the XRP6272 is perfectly suited for powering RF circuitries. Optimized for use with small low cost ESR ceramic output capacitors and featuring a low 30µA quiescent current, this device is also adequate for use in battery powered portable equipments. The XRP6272 operates by default as a 5V fixed output voltage regulator while usage of an external resistors divider allows adjustable out voltages as low as 0.7V. An Enable function, Power Good flag and output noise reduction pin complete the feature set.

Built-in current limit and thermal protections insure safe operations under abnormal operating conditions.

The XRP6272 is offered in RoHS compliant, "green"/halogen free 5-pin TO-252 and 8-pin exposed pad SOIC packages.

APPLICATIONS

- **Networking Equipments**
- **RF Circuitry Power Supplies**
- **Set-top box Equipments**
- **Portable Equipments**

FEATURES

- **Guaranteed 2A Output Current**
  - Low 550mV Dropout at 3.3V/2A
- **1.8V to 6V Single Input Voltage Range**
  - Fixed 5V and Adjustable Output Voltage
  - ±2% Output Voltage Accuracy
- **30µA Quiescent Current**
- **Power Good and Enable Functions**
- **70dB Power Supply Rejection Ratio**
- **Low Output Noise**
- **0.01µA Shutdown Current**
- **Current Limit and Thermal Protection**
- **RoHS compliant "Green"/Halogen Free 5-pin TO-252 and 8-pin Exposed pad SOIC Packages**

TYPICAL APPLICATION DIAGRAM

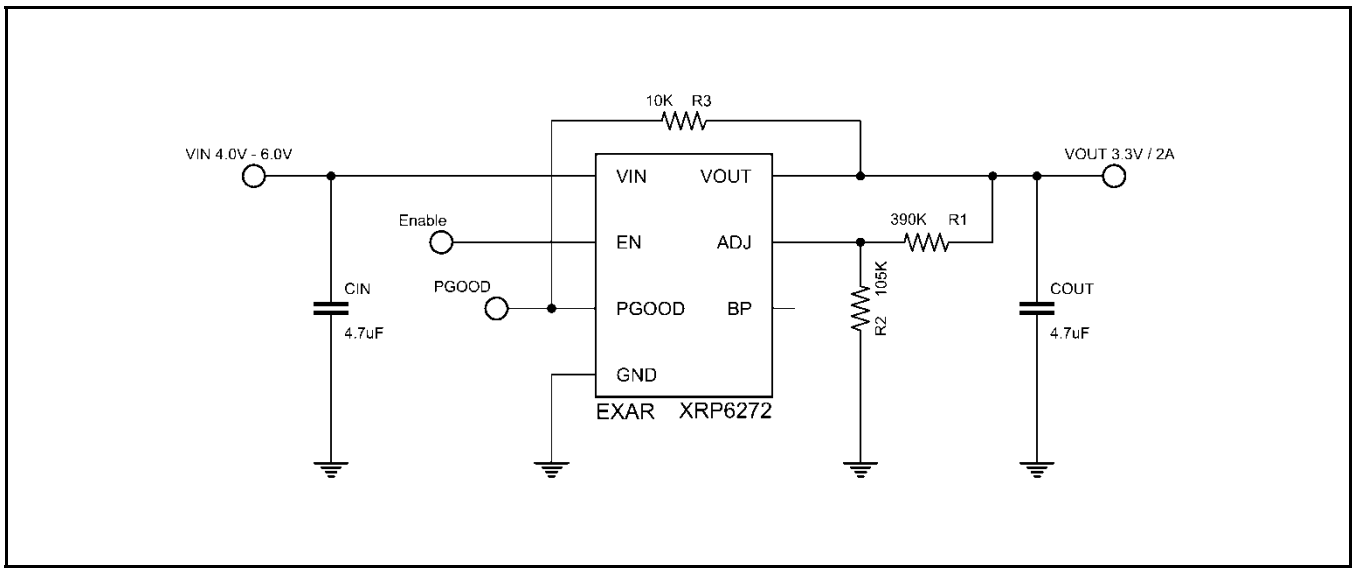


Fig. 1: XRP6272 Application Diagram

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{IN}, EN, BP 7.0V
Storage Temperature ..... -65°C to 150°C
Power Dissipation ..... Internally Limited
Lead Temperature (Soldering, 10 sec) ..... 260°C
Junction Temperature ..... 150°C
ESD Rating (HBM - Human Body Model) 2kV
ESD Rating (MM - Machine Model) 500V

OPERATING RATINGS

Input Voltage Range V_{IN} ..... 1.8V to 6V
Operating Temperature Range ..... -40°C to 85°C
Thermal Resistance
θ_{JA} (5-Pin TO-252) ..... 100°C/W
θ_{JC} (5-Pin TO-252) ..... 8°C/W
θ_{JA} (8-pin HSOIC) ..... 60°C/W
θ_{JC} (8-pin HSOIC) ..... 15°C/W

ELECTRICAL SPECIFICATIONS

Specifications with standard type are for an Operating Junction Temperature of T_J = 25°C only. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN} = V_{OUT} + 1V, C_{IN} = 4.7µF, C_{OUT} = 4.7µF or 10µF (Note 1), C_{BYP} = 22nF, T_J = 25°C.

Parameter	Min.	Typ.	Max.	Units	Conditions
Input Voltage	1.8		6.0	V	
Output Voltage Tolerance	-2		+2	%	I_{OUT} = 1mA
Continuous Output Current	2			A	$V_{IN} \geq$ 2.3V
Ground Current		30	50	µA	$V_{EN} \geq$ 1.6V, No Load
		30	50		$V_{EN} \geq$ 1.6V, I_{OUT} = 300mA
Standby Current		0.01	0.5	µA	V_{EN} = 0
Line Regulation		3	15	mV	V_{IN} = V_{OUT} + 1V to 6V, I_{OUT} =1mA
Load Regulation		5	15	mV	I_{OUT} =1mA to 2A
Output Current Limit	2.2	3.0	3.9	A	
Current Fold Back		1.0		A	
Dropout Voltage (Note 2)		960		mV	I_{OUT} = 2A, V_{OUT} =1.2V
		700	900		I_{OUT} = 2A, V_{OUT} =1.8V
		550	700		I_{OUT} = 2A, V_{OUT} =3.3V
		480	600		I_{OUT} = 2A, V_{OUT} =5.0V
Reference Voltage Tolerance	0.686	0.7	0.714	V	
ADJ Pin Current		10	100	nA	V_{ADJ} = V_{REF}
ADJ Pin Threshold	0.05	0.1	0.2	V	
Enable Turn-On Threshold	1.6			V	Output ON
Enable Turn-Off Threshold			0.4	V	Output OFF
Shutdown Pin Current		0	0.5	µA	V_{EN} = 0
Shutdown Exit Delay Time		100		µs	
Max Output Discharge Resistance to GND during Shutdown		20	100	Ω	
PGOOD Rise Threshold		90	93	%	
PGOOD Hysteresis	3	10		%	
PGOOD Delay	0.5		5	ms	
PGOOD Sink Capability		0.2	0.4	V	I_{PGOOD} = 10mA
Ripple Rejection		70		dB	f=1KHz, Ripple=0.5Vp-p
Output Noise Voltage		24		µVrms	C_{BP} = 22nF, f=10Hz ~100KHz
Temperature Coefficient		50		ppm/°C	
Thermal Shutdown Temperature		150		°C	V_{IN} = V_{OUT} + 1V
Thermal Shutdown Hysteresis		20		°C	

Note 1: In the case of $V_{OUT} \leq 1.8V$, $C_{OUT} = 10\mu F$ is recommended.
Note 2: Dropout Voltage is defined as input voltage minus output voltage when the output voltage drops by 1% of its nominal value at $V_{IN} = V_{OUT} + 1V$.
Note 3: $V_{IN\ (min)}$ is the higher value of (V_{OUT} + Dropout Voltage) or 1.8V.

BLOCK DIAGRAM

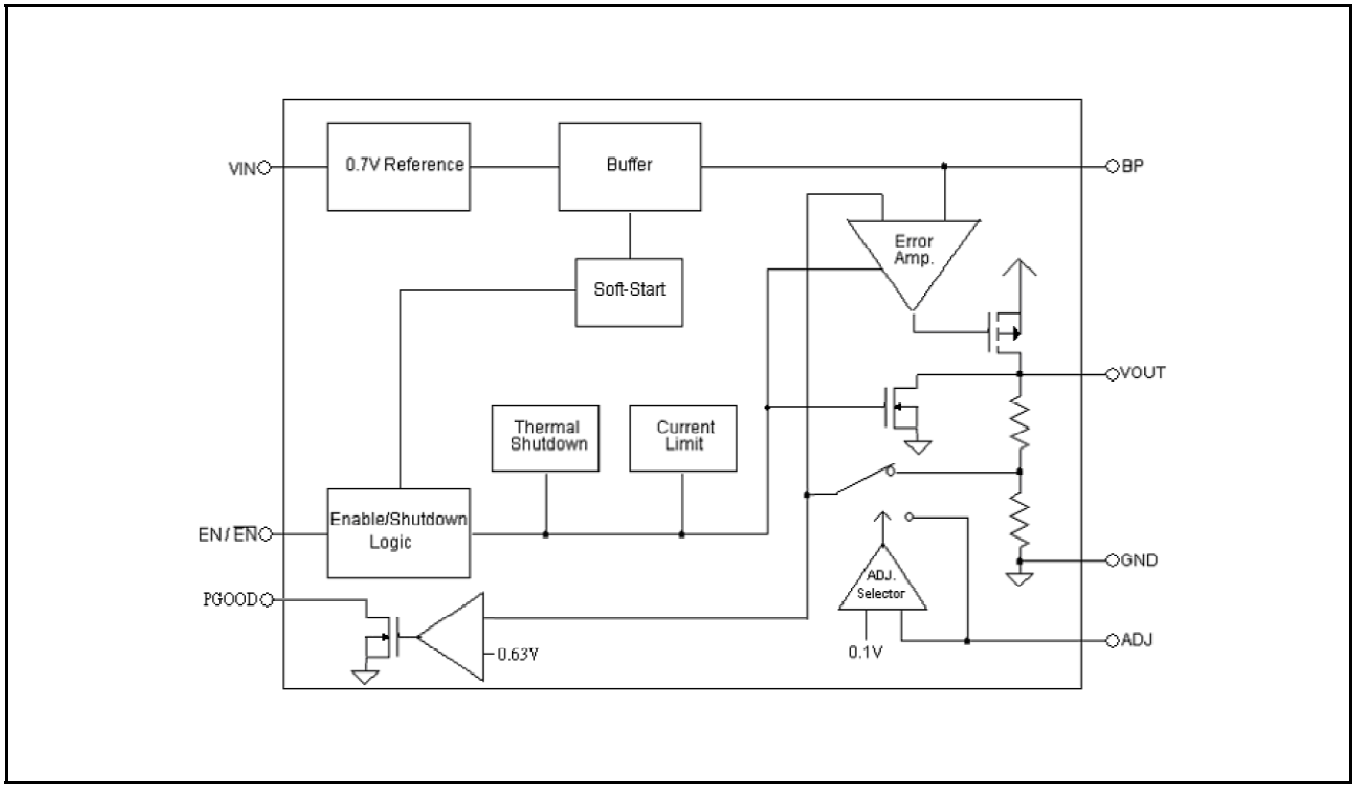


Fig. 2: XRP6272 Block Diagram

PIN ASSIGNMENT

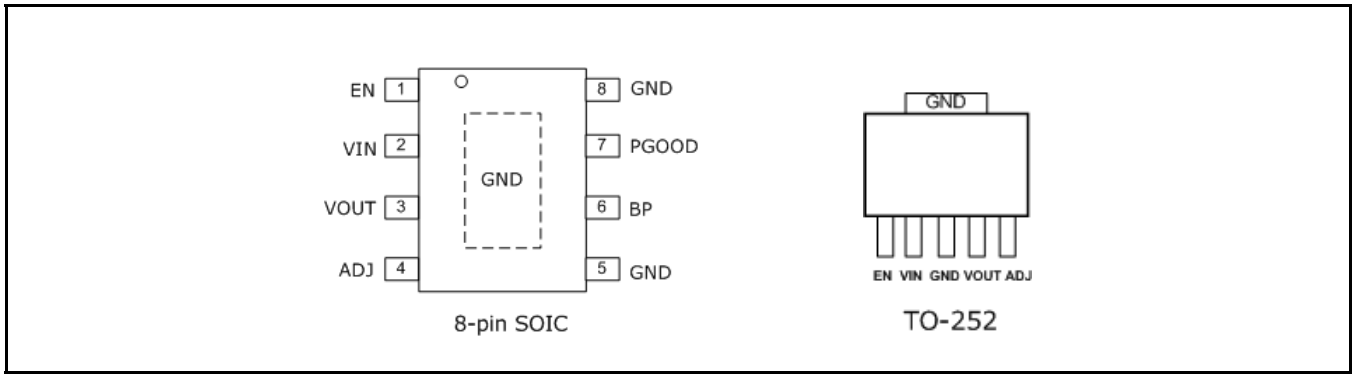


Fig. 3: XRP6272 Pin Assignment

PIN DESCRIPTION

Name	SOIC-8	TO-252	Description
EN	1	1	Enable Pin. Minimum 1.6V to enable the device. Maximum 0.4V to shutdown the device.
VIN	2	2	Power Input Pin. Must be closely decoupled to GND pin with a 4.7µF or greater ceramic capacitor.
VOUT	3	4	Regulator Output pin.
ADJ	4	5	Adjustable Pin. Output Voltage can be set by external feedback resistors when using a resistive divider. Or, connect ADJ to GND for VOUT = 5V, set by internal feedback resistors.
GND	5, 8	3	Ground Signal
BP	6	-	Bypass pin. Connect a 22nF capacitor to GND to reduce output noise. Bypass pin can be left floating if not necessary.
PGOOD	7	-	Power Good open Drain Output.
GND	Exposed Pad	Tab	Connect to GND.

ORDERING INFORMATION

Part Number	Temperature Range	Marking	Package	Packing Quantity	Note 1	Note 2
XRP6272ITC5TR-F	-40°C≤T_A≤+85°C	EXAR XRP6272ITC5 YYWWF X	5-pin TO-252	2K/Tape & Reel	RoHS Compliant Halogen Free	
XRP6272IDBTR-F	-40°C≤T_A≤+85°C	XRP6272I YYWWF XXXX	8-pin HSOIC	2.5K/Tape & Reel	RoHS Compliant Halogen Free	

"YY" = Year – "WW" = Work Week – "X" = Lot Number; when applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at V_{IN} = V_{OUT} + 1V, T_J = T_A = 25°C, C_{IN} = 4.7µF, C_{OUT} = 4.7µF or 10µF (Note 1) unless otherwise specified.

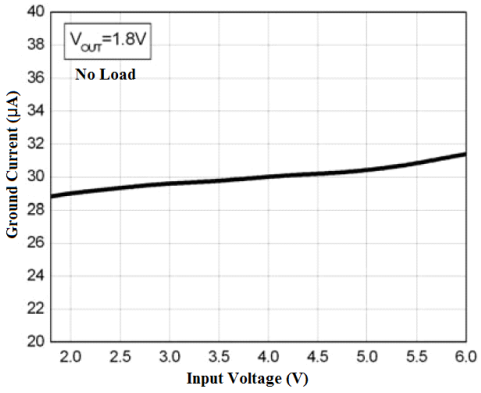


Fig. 4: GND Current vs. VIN at VOUT=1.8V, No Load

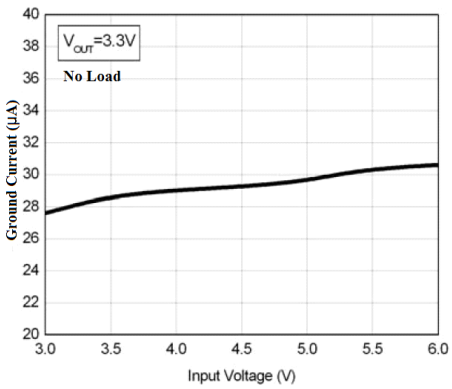


Fig. 5: GND Current vs. VIN at VOUT=3.3V, No Load

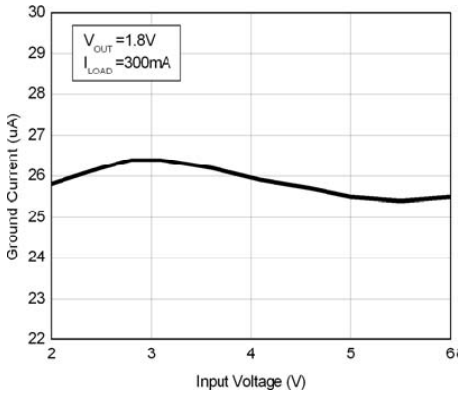


Fig. 6: GND Current vs. VIN at VOUT=1.8V, 300mA

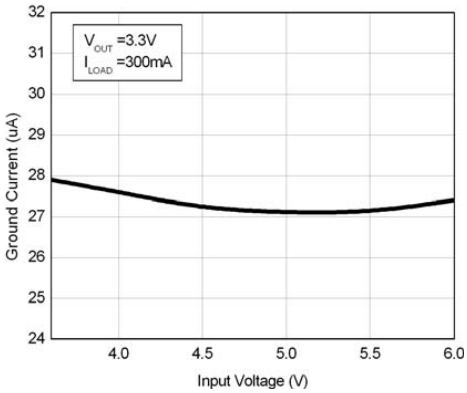


Fig. 7: GND Current vs. VIN at VOUT=3.3V, 300mA

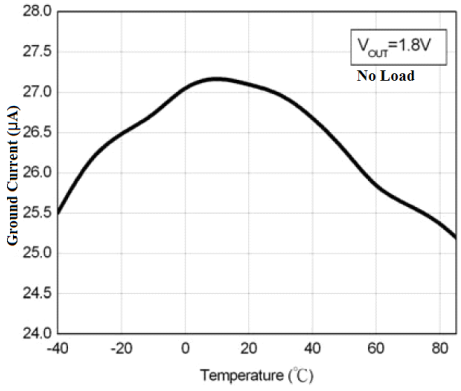


Fig. 8: GND Current vs. Temp. at VOUT=1.8V, No Load

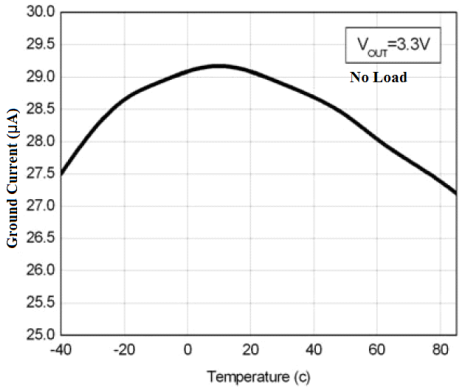


Fig. 9: GND Current vs. Temp. at VOUT=3.3V, No Load

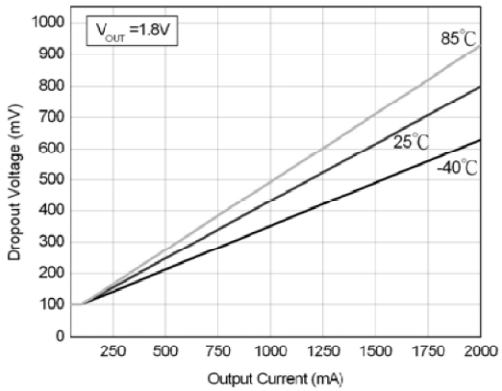


Fig. 10: Dropout Voltage at VOUT = 1.8V

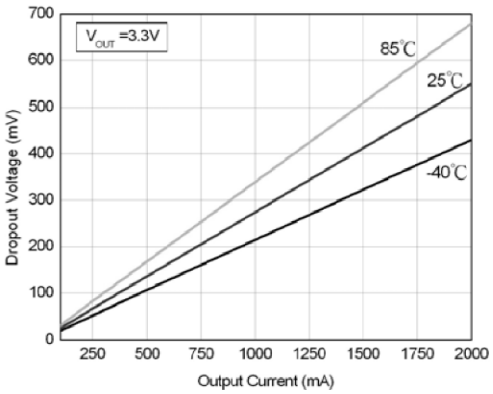


Fig. 11: Dropout Voltage at VOUT = 3.3V

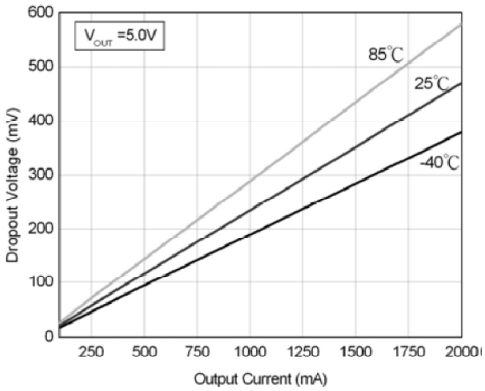


Fig. 12: Dropout Voltage at VOUT = 5.0V

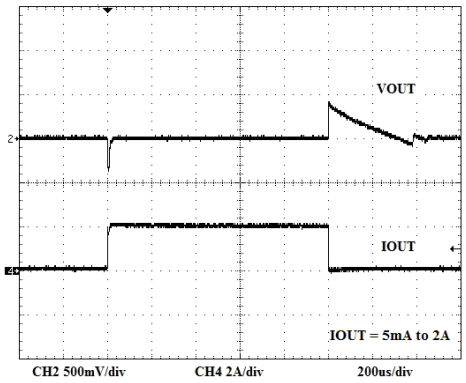


Fig. 13: Load Transient Response at VOUT=1.8V, VIN=2.8V

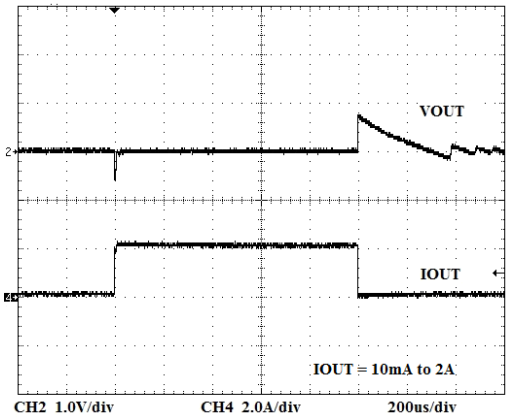


Fig. 14: Load Transient Response at VOUT=3.3V, VIN=4.3V

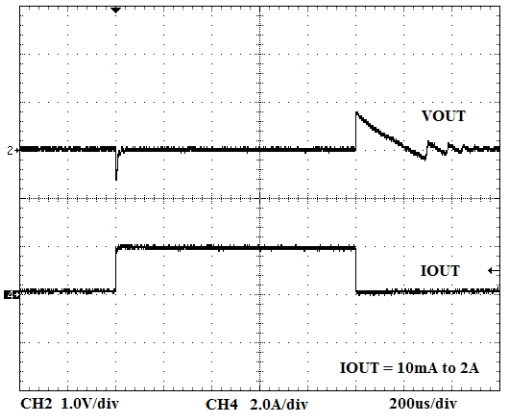


Fig. 15: Load Transient Response at VOUT=5V, VIN=6V

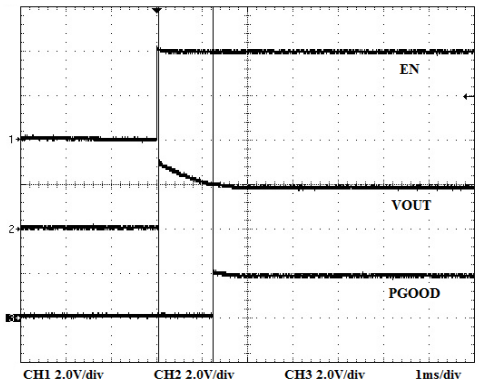


Fig. 16: Enable Startup at VOUT = 1.8V

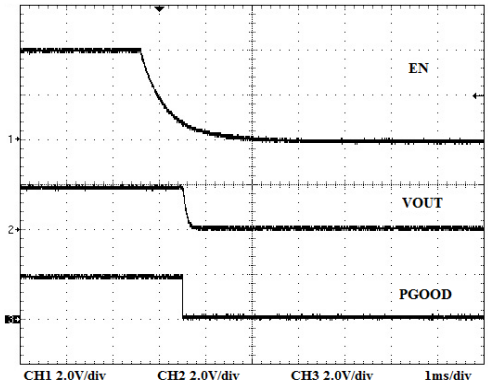


Fig. 17: Shutdown at VOUT = 1.8V

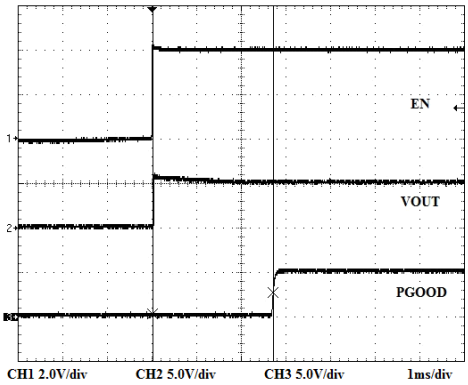


Fig. 18: Enable Startup at VOUT = 5V

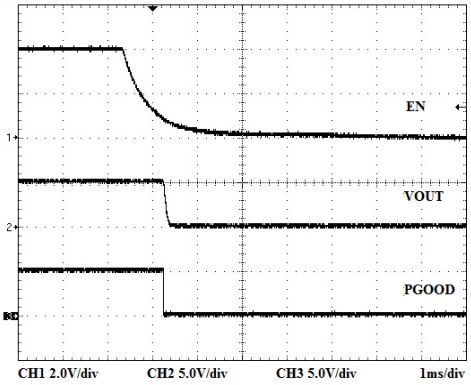


Fig. 19: Shutdown at VOUT = 5V

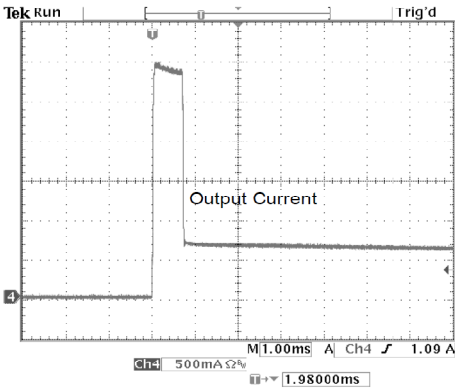


Fig. 20: Current Foldback at VOUT = 1.8V

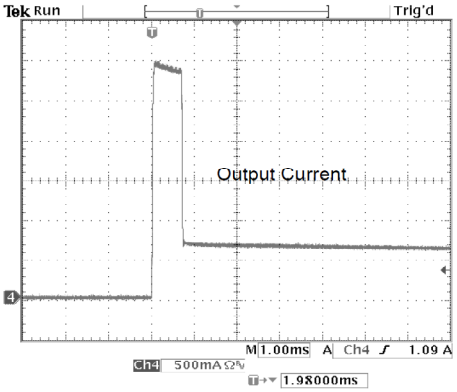


Fig. 21: Current Foldback at VOUT = 3.3V

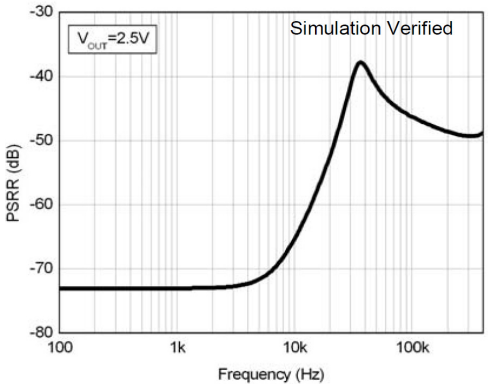
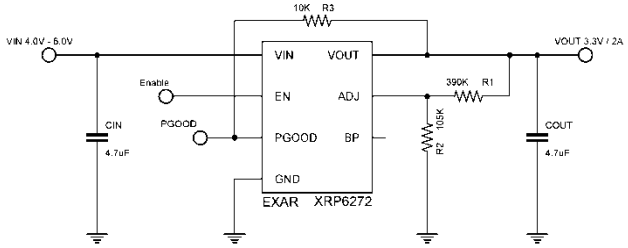


Fig. 22: PSRR Curve

APPLICATION INFORMATION

The XRP6272 is a low-dropout voltage regulator with low quiescent current, low noise and high PSRR. It can support load current up to 2A. It incorporates current-limit and thermal protection features.

TYPICAL APPLICATION SCHEMATIC



PROGRAMMING THE OUTPUT VOLTAGE

XRP6272's internal feedback resistors set the output voltage V_{OUT} to 5V when the ADJ pin is connected to GND. Alternatively; the output voltage is adjustable via the external feedback resistor network R1 and R2 by calculating the following formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where, V_{REF} is the reference voltage set internally at 0.7V nominal.

INPUT & OUTPUT CAPACITORS

XRP6272 is optimized for use with ceramic capacitors. To ensure stability of the device, an output ceramic capacitor of at least 4.7µF or 10µF (for $V_{OUT} \leq 1.8V$) is recommended. An input capacitor of 4.7µF is recommended.

X5R or X7R ceramic capacitors are recommended as they have the best temperature and voltage characteristics.

NOISE BYPASS CAPACITOR

A 22nF bypass capacitor at BP pin can reduce output voltage noise. This pin can be left floating if it is unnecessary.

THEORY OF OPERATION

SHUTDOWN

By connecting EN pin to GND, the XRP6272 can be shutdown to reduce the supply current to 0.01µA (typ.). In this mode, the output voltage of XRP6272 is equal to 0V.

CURRENT LIMIT

The XRP6272 includes current limit protection feature, which monitors and controls the maximum output current. If the output is overloaded or shorted to ground, this can protect the device from being damaged.

THERMAL PROTECTION

The XRP6272 includes a thermal protection feature that protects the IC by turning off the pass transistor when the maximum junction temperature T_J exceeds 150ºC.

POWER DISSIPATION

The power dissipation across the device can be calculated as:

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT})$$

The total junction temperature is calculated as:

$$T_J = T_A + P_D \times \theta_{JA}$$

where, T_J is the junction temperature, T_A is the ambient temperature and Θ_{JA} is the thermal resistance between junction to ambient.

There is a temperature rise associated with this power dissipated while operating in a given ambient temperature. If the calculated junction temperature exceeds maximum junction temperature specification, then the built-in thermal protection feature is triggered as described previously.

To insure reliable performance, the maximum allowable power dissipation for a given ambient temperature must be considered and it can be calculated as follows:

$$P_{D(MAX)} = (T_{J(MAX)} - (T_A))/\theta_{JA}$$

where, $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature and Θ_{JA} is the thermal resistance between junction to ambient. In order to insure the best thermal flow, proper mounting of the IC is required.

LAYOUT CONSIDERATION

1. Connect the bottom-side pad to a large ground plane for good thermal conductivity and to reduce the thermal resistance of the device.

2. The input capacitor C_{IN} and output capacitor C_{OUT} must be placed as close as possible to the pins V_{IN} and V_{OUT} respectively.

3. Use short wires to connect the power supply to pins V_{IN} and GND on the board.

TYPICAL APPLICATIONS

APPLICATION 1

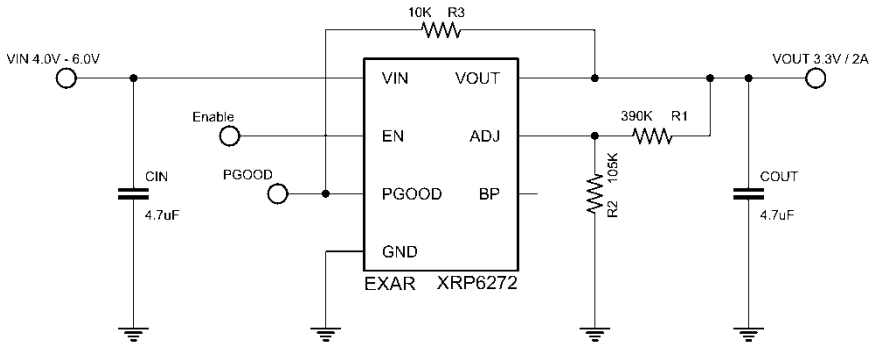


Fig. 23: 5V to 3.3V / 2A

APPLICATION 2

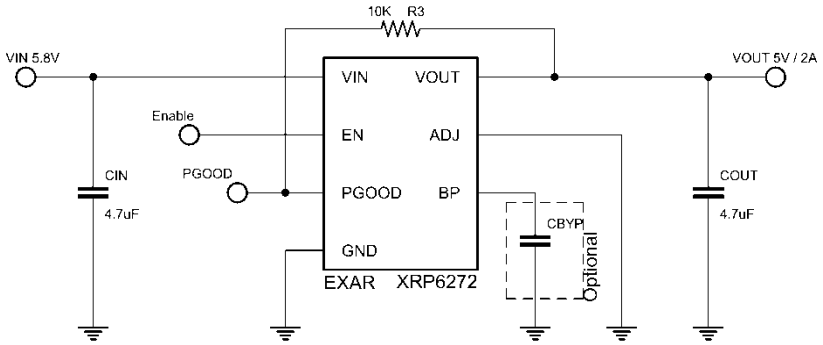


Fig. 24: 5.8V to 5V RF Stage Low Noise Power Supply

APPLICATION 3

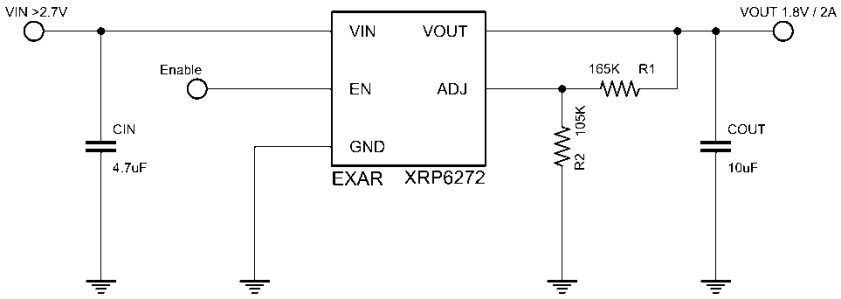
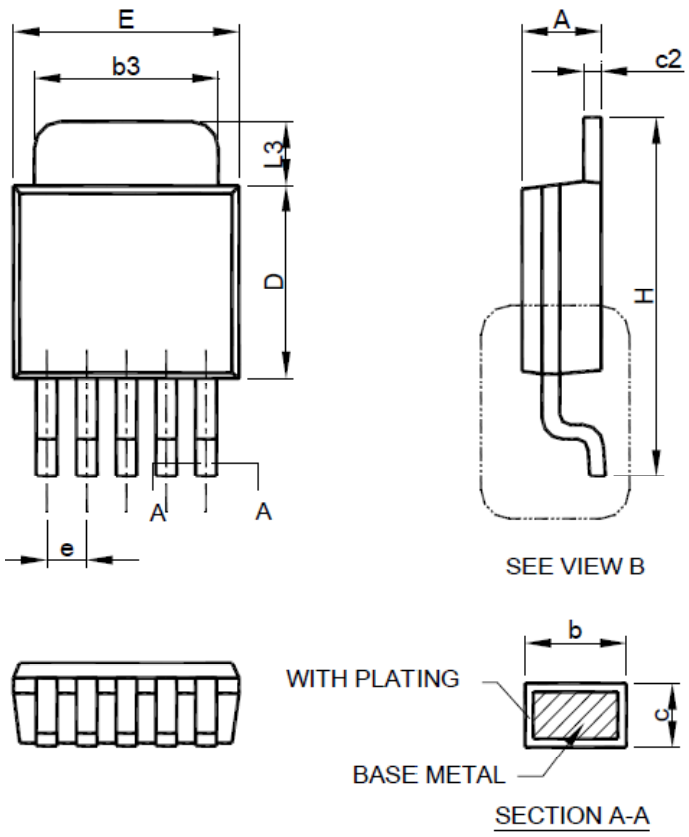


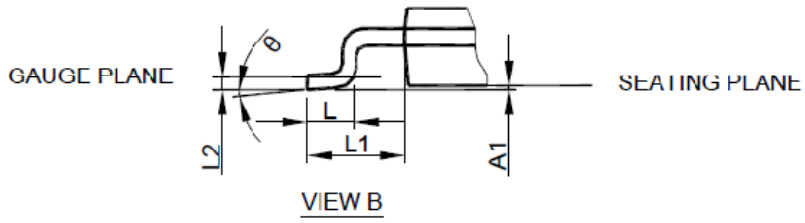
Fig. 25: 2.7V Min to 1.8V / 2A Power Supply

PACKAGE SPECIFICATION

TO-252-5L

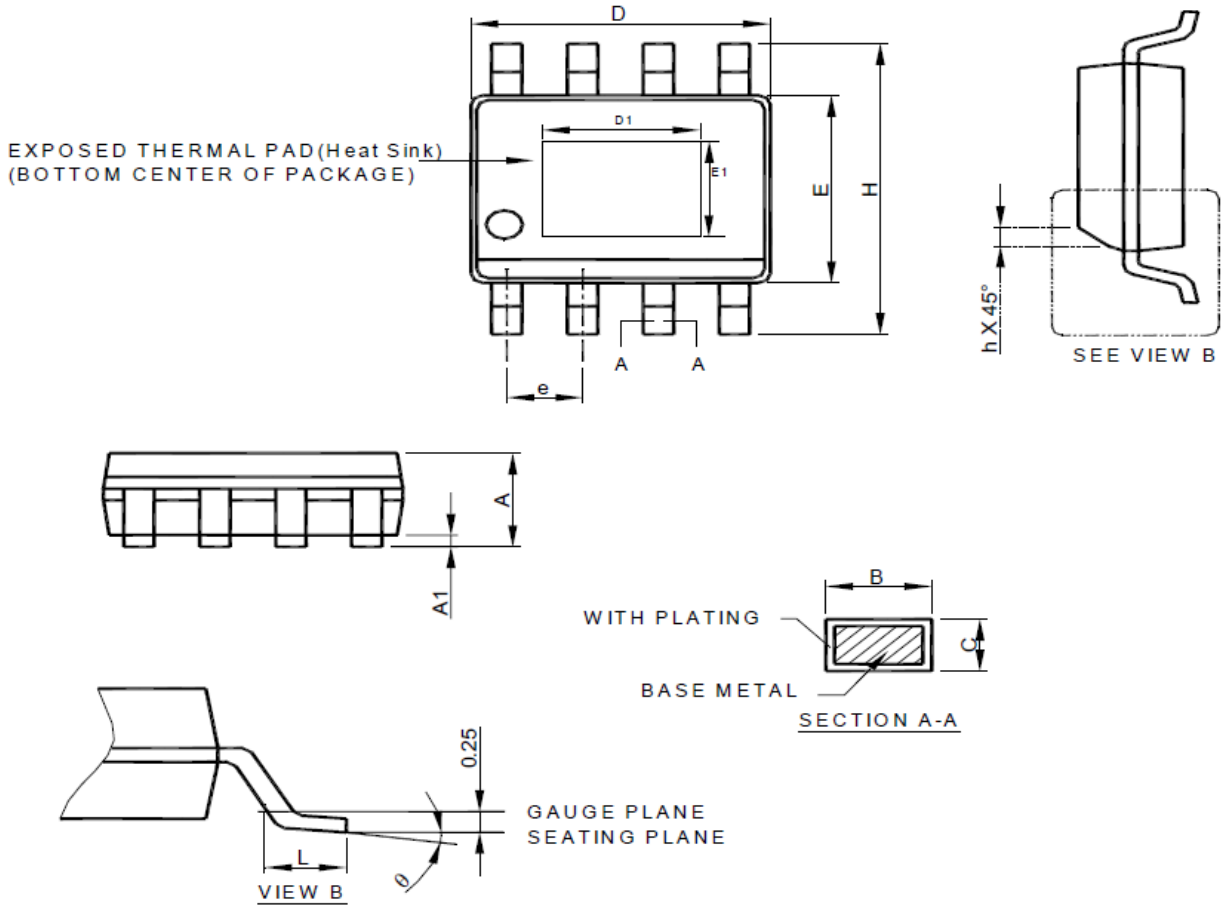


SYMBOL	TO-252-5L	
	MILLIMETERS	
	MIN.	MAX.
A	2.19	2.38
A1	0.00	0.13
b	0.51	0.71
b3	4.32	5.46
c	0.46	0.61
c2	0.46	0.89
D	5.33	6.22
E	6.35	6.73
e	1.27 BSC	
H	9.40	10.41
L	1.40	1.78
L1	2.67 REF	
L2	0.51 BSC	
L3	0.89	2.03
q	0°	8°



Note: 1. Refer to JEDEC TO-252AD and AB.
2. Dimension "E" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "D" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

EXPOSED PAD 8-PIN SOIC



SYMBOL	SOP-8 Exposed Pad(Heat Sink)	
	MILLIMETERS	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.15
B	0.31	0.51
C	0.17	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
q	0°	8°
D1	1.5	3.5
E1	1.0	2.55

Note : 1. Refer to JEDEC MS-012E.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

REVISION HISTORY

Revision	Date	Description
1.1.0	10/14/2011	Initial release of Data Sheet
1.2.0	11/30/2011	Corrected pin assignment package drawing

FOR FURTHER ASSISTANCE

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