24-bit Capacitance to Digital Converter with Temperature Sensor

Preliminary Technical Data

AD7747

FEATURES

Capacitance to Digital Converter (CDC)
- **Standard One Chip Solution**
- **Interfaces to Single or Differential Grounded Sensors**
- **Resolution: 40 aF (i.e. 18-bit) at 16.6 Hz**
- **Accuracy: 4 fF**
- **Linearity: 0.01%**
- **Input Range: ±8 pF**
- **Offset / Common Capacitance Removal: up to 17 pF**
- **Update rate: 5 Hz to 90 Hz**
- **Simultaneous 50 Hz and 60 Hz rejection at 16.6 Hz**
- **Tolerant of ground capacitance and ground leakage current**

Temperature sensor on chip
- **Resolution: 0.1°C, accuracy: ±2°C**

Voltage input channel

Internal clock oscillator

2-Wire Serial Interface (I²C®-Compatible)

Power
- **2.7 V to 5.25 V Single-Supply Operation**
- **1 mA Current Consumption**

Operating temperature: -40°C to +125°C

Package: 16-lead TSSOP

APPLICATIONS

Automotive, Industrial and Medical Systems for:
- **Pressure Measurement**
- **Position Sensors**
- **Level Sensors**
- **Flowmeters**
- **Humidity Sensors**
- **Impurity Detection**

GENERAL DESCRIPTION

The AD7747 is a high-resolution Σ–Δ capacitance to digital converter (CDC). The capacitance to be measured is connected directly to the device inputs. The architecture features inherent high resolution (24-bit no missing codes, 18-bit effective resolution at 16.6 Hz data rate), high linearity (±0.01%) and high accuracy (±4 fF factory calibrated). The AD7747 capacitance input range is ±8 pF (changing), while it can accept up to 17 pF absolute capacitance (not changing), which is compensated by an on-chip digital to capacitance converter (CAPDAC).

The AD7747 is designed for single ended or differential capacitive sensors with one plate connected to ground. For floating capacitive sensors, the AD7745 or AD7746 are recommended.

The part has an on-chip temperature sensor with resolution of 0.1°C and accuracy of ±2°C. The on-chip voltage reference and the on-chip clock generator eliminate the need for any external components in most capacitive sensor applications. The part has a standard voltage input, which together with the differential reference input allows easy interface to an external temperature sensor, such as an RTD, thermistor or diode.

The AD7747 has a 2-wire, I²C compatible serial interface. The part operates from a single 3 V or 5 V power supply. It is specified over the automotive temperature range of -40°C to +125°C and is housed in a 16-lead TSSOP package.

FUNCTIONAL BLOCK DIAGRAMS

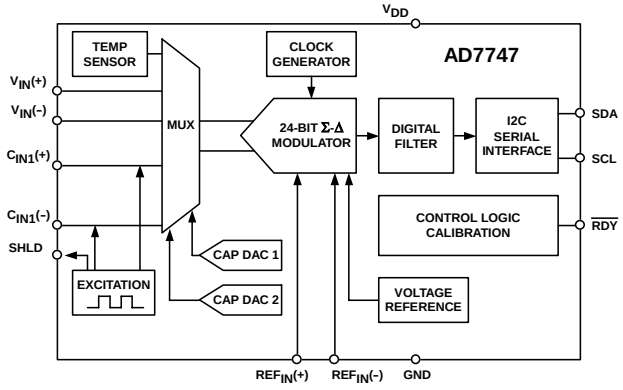

Figure 1.

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TABLE OF CONTENTS

AD7747—PRELIMINARY SPECIFICATIONS

Table 1. (V_{DD} = 2.7 V to 3.3 V, or 4.75V to 5.25V, GND = 0 V, –40°C to +125°C, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CAPACITIVE INPUT (INPUTS)					
Conversion Input Range		±8.192		pF	Factory calibrated
Integral Nonlinearity (INL) [1]			±0.01	% of FSR	
No-missing Codes [1]	24			bit	62ms conversion time
Resolution p-p		16		bit	62ms conversion time
Resolution effective		18		bit	62ms conversion time
Output Noise rms		10		aF/√Hz	62ms conversion time
Absolute Error [2]			±4	fF	25°C, after offset calibration 62ms conversion time
Offset Error		TBD		aF	After system offset calibration
Offset Drift vs. Temperature		TBD		fF/°C	
Gain Error		TBD		% of FS	
Gain Drift vs. Temperature [1]		-27		ppm of FS/°C	
Power Supply Rejection		TBD		fF/V	
Conversion Time	22.0		219.2	ms	Configurable via digital interface
CAPDAC					
Full Range	17	21		pF	
Resolution [3]		330		fF	6-bit CAPDAC
Drift vs. Temperature [1]		+27		ppm of FS/°C	
EXCITATION					
Frequency		16		kHz	
Voltage across Capacitance		± V_{DD} /8		V	Configurable via digital interface
		± V_{DD} /4		V	
		± V_{DD} × 3/8		V	
		± V_{DD} /2		V	
ACTIVE SHIELDING					SHLD pin
Allowed Capacitance to GND [1]			50	pF	
TEMPERATURE SENSOR [4]					VTCHOP [4] = 1
Resolution		0.1		°C	
Error [1]		±0.5	±2	°C	Internal temperature sensor
		±2	±4	°C	External sensing diode
VOLTAGE INPUT [4]					
Differential VIN Voltage Range		±V_{REF}		V	
Absolute VIN Voltage	GND –0.03		V_{DD} +0.03	V	
Integral Nonlinearity (INL) [1]		±5	±15	ppm of FSR	
No-missing Codes [1]	24			bit	62ms conversion time
Resolution p-p		16		bits	62ms conversion time
Output Noise		3		µV rms	62ms conversion time
Offset Error		±3		µV	
Offset Drift vs. Temperature		15		nV/°C	
Full-Scale Error [5]		±10		µV	
Full-Scale Drift vs. Temperature		TBD		ppm of FSR/°C	External reference
Average VIN Input Current		400		nA/V	
Analog VIN Input Current Drift		±50		pA/V/°C	
Power Supply Rejection		90		dB	External reference
Power Supply Rejection		80		dB	Internal reference
Common-Mode Rejection		90		dB	
Conversion Time	20.1		122.1	ms	Configurable via Digital Interface

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INTERNAL VOLTAGE REFERENCE					
Voltage	1.168	1.17	1.172	V	At V_{DD} = 4V, T_A = 25°C
Drift vs. Temperature		10		ppm/°C	
EXTERNAL VOLTAGE REFERENCE INPUT					
Differential REFIN Voltage [1]	0.1	2.5	V_{DD}	V	
Absolute REFIN Voltage	GND –0.03		V_{DD} +0.03	V	
Average REFIN Input Current		±400		nA/V	
Average REFIN Input Current Drift		±50		pA/V/°C	
SERIAL INTERFACE					
LOGIC INPUTS (SCL, SDA)					
V_{IH} Input High Voltage	2.1			V	
V_{IL} Input Low Voltage			0.8	V	
Hysteresis		150		mV	
OPEN-DRAIN OUTPUT (SDA)					
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = –6.0 mA
I_{OH} Output High Leakage Current		0.1	1	µA	V_{OUT} = V_{DD}
LOGIC OUTPUT ($\overline{RDY}$)					
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = 1.6 mA, V_{DD} = 5 V
V_{OH} Output High Voltage	4.0			V	I_{SOURCE} = 200 µA, V_{DD} = 5 V
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = 100 µA, V_{DD} = 3 V
V_{OH} Output High Voltage	DV_{DD} – 0.6			V	I_{SOURCE} = 100 µA, V_{DD} = 3 V
POWER REQUIREMENTS					
V_{DD} to GND Voltage	4.75		5.25	V	V_{DD} = 5 V nominal
	2.7		3.3	V	V_{DD} = 3 V nominal
I_{DD} Current			1	mA	Digital inputs equal to V_{DD} or GND
I_{DD} Current Power Down Mode		1		µA	Digital inputs equal to V_{DD} or GND

[1] Specification is not production tested, but is supported by characterization data at initial product release.
[2] Factory calibrated The absolute error includes factory gain calibration error, integral nonlinearity error, and offset error after system offset calibration, all at 25°C. At different temperatures, compensation for gain drift over temperature is required.
[3] The CAPDAC resolution is 6-bit in the actual CAPDAC full range. Using the on-chip offset calibration or adjusting the capacitive offset calibration register can further reduce the CIN offset or the non-changing CIN component.
[4] The VTCHOP bit in the VT SETUP register must be set to 1 for the specified temperature sensor and voltage input performance.
[5] Full-scale error applies to both positive and negative full-scale.

TIMING SPECIFICATIONS

Table 2. (V_{DD} = 2.7 V to 3.3 V, or 4.75V to 5.25V, GND = 0 V; Input Logic 0 = 0 V; Input Logic 1 = V_{DD}; –40°C to +125°C, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL INTERFACE[1, 2]					See Figure 2
SCL Frequency	0		400	kHz	
SCL High Pulse Width, t_{HIGH}	0.6			µs	
SCL Low Pulse Width, t_{LOW}	1.3			µs	
SCL, SDA Rise Time, t_R			0.3	µs	
SCL, SDA Fall Time, t_F			0.3	µs	
Hold Time (Start Condition), $t_{HD;STA}$	0.6			µs	After this period, the first clock is generated
Setup Time (Start Condition), $t_{SU;STA}$	0.6			µs	Relevant for repeated start condition
Data Setup Time, $t_{SU;DAT}$	0.1			µs	
Setup Time (Stop Condition), $t_{SU;STO}$	0.6			µs	
Data Hold Time, $t_{HD;DAT}$ (Master)	0			µs	
Bus Free Time (Between Stop and Start Condition, t_{BUF}	1.3			µs	

[1] Sample tested during initial release to ensure compliance.
[2] All input signals are specified with input rise/fall times = 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Output load = 10 pF.

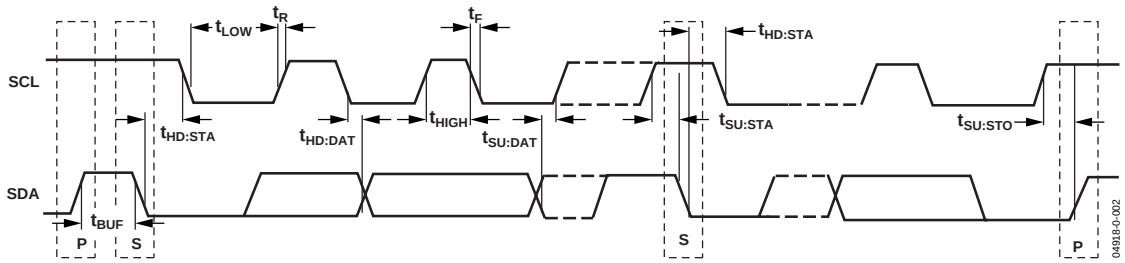

Figure 2.Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3. (T_A = 25°C, unless otherwise noted.)

Parameter	Rating
Positive Supply Voltage V_{DD} to GND	–0.3 V to +6.5 V
Voltage on any input or output pin to GND	–0.3 V to V_{DD} + 0.3 V
ESD Rating (ESD Association Human Body Model, S5.1)	TBD V
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
TSSOP Package θ_{JA} Thermal Impedance to Air	128 °C/W
TSSOP Package θ_{JC} Thermal Impedance to Case	14 °C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

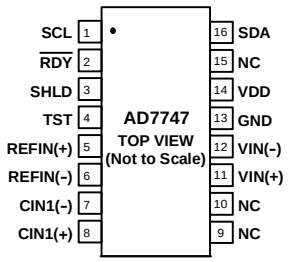

Figure 3. AD7747 Pin Configuration (16-Lead TSSOP)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCL	Serial interface clock input. Connects to the master's clock line. (Requires pull-up resistor if not already provided in the system.)
2	$\overline{RDY}$	Logic output. A falling edge on this output indicates that a conversion on enabled channel(s) has been finished and the new data are available. Alternatively, the status register can be read via the 2-wire serial interface and the relevant bit(s) decoded to query finished conversion. If not used, this pin should be left open circuit.
3	SHLD	Capacitive input active AC shielding. To eliminate the CIN parasitic capacitance to ground, the SHLD signal can be used to for shielding the connection between the sensor and CIN. See the max allowed capacitance. If not used, this pin must be left open circuit.
4	TST	This pin must be left open circuit for proper operation
5, 6	REFIN(+), REFIN(–)	Differential voltage reference input for the voltage channel (ADC). Alternatively, the on-chip internal reference can be used for the voltage channel. These reference input pins are not used for conversion on capacitive channel(s) (CDC). If not used, these pins can be left open circuit or connected to GND.
7	CIN1(-)	CDC negative capacitive input in differential mode. This pin is internally disconnected in single ended CDC configuration. If not used, this pin must be left open circuit.
8	CIN1(+)	CDC capacitive input (in single ended mode) or positive capacitive input (in differential mode). The measured capacitance is connected between one of the CIN pins and GND. If not used, this pin must be left open circuit.
9, 10	NC	These pins can be left open circuit or connected to GND.
11, 12	VIN(+), VIN(–)	Differential voltage input for the voltage channel (ADC). These pins are also used to connect an external temp sensing diode. If not used, these pins can be left open circuit or connected to GND.
13	GND	Ground pin.
14	V_{DD}	Power supply voltage. This pin should be decoupled to GND, using a low impedance capacitor, for example combination of 10uF tantalum and 0.1uF multilayer ceramic.
15	NC	Not connected. This pin should be left open circuit.
16	SDA	Serial interface bidirectional data. Connects to the master's data line. Requires pull-up resistor if not provided elsewhere in the system.

SERIAL INTERFACE

The AD7747 supports an I2C compatible two wire serial interface. The two wires on the I2C Bus are called SCL, (clock) and SDA, (data). These two wires carry all addressing, control and data information one bit at a time over the bus to all connected peripheral devices. The SDA wire carries the data, while the SCL wire synchronizes the sender and receiver during the data transfer. I2C devices are classified as either a MASTER or SLAVE devices. A device that initiates a data transfer message is called a master, while a device that responds to this message is called a slave.

To control the AD7747 device on the bus the following protocol must be followed. First, the master initiates a data transfer by establishing a START CONDITION, defined by a high-to-low transition on SDA while SCL remains high. This indicates that the START BYTE will follow next. This 8 bit, start byte is made up of a 7 bit address plus an R/W bit indicator.

All peripherals connected to the bus respond to the start condition and shift in the next eight bits (7-bit address + R/W bit). The bits arrive MSB first. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as the ACKNOWLEDGE bit. All other devices withdraw from the bus at this point and maintain an IDLE CONDITION. An exception to this is the GENERAL CALL address which is described later in this document. The idle condition is where the device monitors the SDA and SCL lines waiting for the start condition and the correct address byte. The R/W bit determines the direction of the data transfer. A logic '0' LSB in the start byte means that the master will write information to the addressed peripheral. In this case the AD7747 becomes a slave receiver. A logic '1' LSB in the start byte means that the master will read information from the addressed peripheral. In this case the AD7747 becomes a slave transmitter. In all instances, the AD7747 acts as a standard slave device on the I2C bus.

The start byte address for the AD7747 is 0x90 for a Write and 0x91 for a Read.

WRITE OPERATION

When a WRITE is selected, the byte following the start byte is always the register ADDRESS POINTER (sub-address) byte, which points to of one of the internal registers on the AD7747. The address pointer byte is automatically loaded into the address pointer register and acknowledged by the AD7747. After the address pointer byte acknowledge, a STOP CONDITION, REPEATED START CONDITION, or another data byte can follow from the master.

A stop condition is defined by a low-to-high transition on SDA while SCL remains high. If a stop condition is ever encountered by the AD7747, it will return to its idle condition and the address pointer is reset to address 0x00.

If a data byte is transmitted after the register address pointer byte, the AD7747 will load this byte into the register that is currently addressed by the address pointer register, send an acknowledge and the address pointer auto-incrementer will automatically increment the address pointer register to the next internal register address. Thus subsequent transmitted data bytes will be loaded into sequentially incremented addresses.

If a repeated start condition is encountered after the address pointer byte, all peripherals connected to the bus respond exactly as outlined above for a start condition, i.e. a repeated start condition is treated the same as a start condition. (When a master device issues a stop condition, it relinquishes control of the bus, allowing another master device to take control of the bus. Hence, a master wanting to retain control of the bus will issue successive start conditions known as repeated start conditions).

READ OPERATION

When a READ is selected in the start byte, the register that is currently addressed by the address pointer is transmitted on to the SDA line by the AD7747. This is then clocked out by the master device and the AD7747 will await an acknowledge from the master.

If an acknowledge is received from the master, the address auto-incrementer will automatically increment the address pointer register and output the next addressed registers contents on to the SDA line for transmission to the master. If no acknowledge is received the AD7747 returns to its idle state and the address pointer is not incremented.

The address pointers' auto-incrementer allows block data to be written or read from the starting address and subsequent incremental addresses. The user can also access any unique register (address) on a one-to-one basis without having to update all the registers. The address pointer register contents cannot be read.

If an incorrect address pointer location is accessed or, if the user allows the auto incrementer to exceed the required register address, the following applies:

1. In Read Mode, the AD7747 will continue to output various internal register contents until the master device issues a not-acknowledge, start or stop condition. The address pointers' auto-incrementer's contents will reset to point to the STATUS REGISTER at address 0x00 when a stop condition is received at the end of a read operation. This allows the status register to be read (polled) continually without having to constantly write to address pointer.
2. In Write Mode, the data for the invalid address will not be loaded into the AD7747 registers but an acknowledge will be issued by the AD7747.

GENERAL CALL

When a master issues a slave address consisting of seven zeros with the eighth bit (R/W bit) set to zero, this is known as the general call address. The general call address is for addressing every device connected to the I2C bus. The AD7747 will acknowledge this address and read in the following data byte.

If the second byte is 0x06, the AD7747 will reset completely uploading all default values. The AD7747 will not acknowledge any other general call commands.

AD7747 RESET

In order that the AD7747 can be reset without having to reset the entire I2C bus, an explicit reset command is provided. This uses a particular address pointer word as a command word to reset the part and upload all default settings.

The reset command address word is 0xBF.

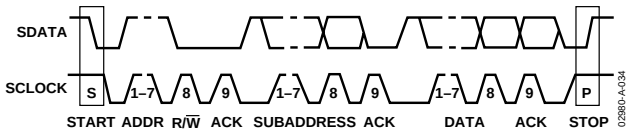

Figure 4. Bus Data Transfer

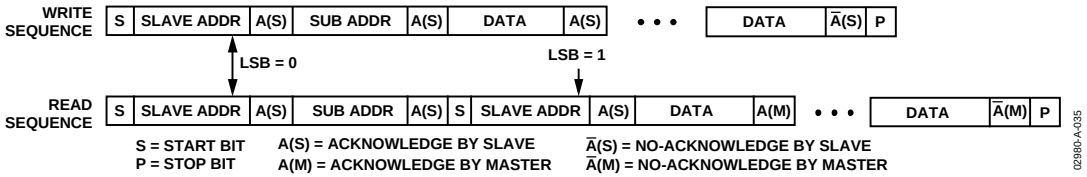

Figure 5. Write and Read Sequences

REGISTER DESCRIPTIONS

The master can write to or read from all of the AD7747 registers except the address pointer register, which is a write-only register. The address pointer register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the address pointer register.

After the part has been accessed over the bus and a read/write operation is selected, the address pointer register is set up. The address pointer register determines to/from which register the operation takes place. A read/write operation is performed from to the target address, which then increments to the next address until a stop command on the bus is performed.

Table 5. Register Summary

Register	Address Pointer		Dir	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	(dec)	(hex)		(Default Value)							
Status	0	0x00	R	-	-	-	-	-	RDY	RDYVT	RDYCAP
				0	0	0	0	0	1	1	1
Cap Data H	1	0x01	R	Capacitive channel data – High byte					0x00		
Cap Data M	2	0x02	R	Capacitive channel data – Middle byte					0x00		
Cap Data L	3	0x03	R	Capacitive channel data – Low byte					0x00		
VT Data H	4	0x04	R	Voltage / Temperature channel data – High byte					0x00		
VT Data M	5	0x05	R	Voltage / Temperature channel data – Middle byte					0x00		
VT Data L	6	0x06	R	Voltage / Temperature channel data – Low byte					0x00		
Cap Setup	7	0x07	R/W	CAPEN	-	CAPDIFF	-	-	-	-	-
				0	0	0	0	0	0	0	0
VT Setup	8	0x08	R/W	VTEN	VTMD1	VTMD0	EXTREF	-	-	VTSHORT	VTCHOP
				0	0	0	0	0	0	0	0
Exc Setup	9	0x09	R/W	CLKCTRL	-	-	-	-	-	EXCLVL1	EXCLVL0
				0	0	0	0	0	0	1	1
Configuration	10	0x0A	R/W	VTFS1	VTFS0	CAPFS2	CAPFS1	CAPFS0	MD2	MD1	MD0
				1	0	1	0	0	0	0	0
Cap DAC A	11	0x0B	R/W	DACAENA	-	DACA – 6-Bit Value					
				0	0	0x00					
Cap DAC B	12	0x0C	R/W	DACBENB	-	DACB – 6-Bit Value					
				0	0	0x00					
Cap Offset H	13	0x0D	R/W	Capacitive offset calibration – High byte					0x80		
Cap Offset L	14	0x0E	R/W	Capacitive offset calibration – Low byte					0x00		
Cap Gain H	15	0x0F	R/W	Capacitive gain calibration – High byte					Factory calibrated		
Cap Gain L	16	0x10	R/W	Capacitive gain calibration – Low byte					Factory calibrated		
Volt Gain H	17	0x11	R/W	Voltage gain calibration – High byte					Factory calibrated		
Volt Gain L	18	0x12	R/W	Voltage gain calibration – Low byte					Factory calibrated		

STATUS REGISTER

Address pointer 0x00, read only, default value 0x07

Indicates status of the converter. Status register can be read via the 2-wire serial interface to query a finished conversion.

The $\overline{RDY}$ pin reflects status of the RDY bit. Therefore, the $\overline{RDY}$ pin high to low transition can be used as an alternative indication of the finished conversion.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	-	-	-	-	-	RDY	RDYVT	RDYCAP
Default	0	0	0	0	0	1	1	1

Bit	Mnemonic	Description
7-3	-	Not used, always read 0
2	RDY	RDY = 0 indicates that conversion on the enabled channel(s) has been finished and new unread data are available. If both capacitive and voltage / temperature channels are enabled, thy RDY bit will be changed to 0 after conversion on both channels is finished. The RDY bit will return to 1 either when data are read or prior finishing the next conversion. If only one channel is enabled, for example capacitive, then the RDY bit will reflect the RDYCAP bit.
1	RDYVT	RDYVT = 0 indicates that a conversion on the voltage / temperature channel has been finished and new unread data are available.
0	RDYCAP	RDYCAP = 0 indicates that a conversion on the capacitive channel has been finished and new unread data are available.

CAP DATA REGISTER

24 bits, address pointer 0x01, 0x02, 0x03, read only, default value 0x000000

Capacitive channel output data. The register is updated after finished conversion on the capacitive channel, with one exception: When the serial interface read operation from the CAP DATA register is in progress, the data register is not updated and the new capacitance conversion result is lost.

Stop condition on the serial interface is considered as the end of the read operation. Therefore, to prevent data corruption, all 3 bytes of the data register should be read subsequently using the register address pointer auto-increment feature of the serial interface.

To prevent losing some of the results, the CAP DATA register should be read before the next conversion on the capacitive channel is finished.

Code 0x000000 represents negative full-scale (-8.192 pF), code 0x800000 represents zero scale (0 pF) and the code 0xFFFFFF represents positive full scale (+8.192 pF).

VT DATA REGISTER

24 bits, address pointer 0x04, 0x05, 0x06, read only, default value 0x000000

Voltage / Temperature channel output data. The register is updated after finished conversion on the voltage channel or temperature channel, with one exception: When the serial interface read operation from the VT DATA register is in progress, the data register is not updated and the new voltage / temperature conversion result is lost.

Stop condition on the serial interface is considered as the end of the read operation. Therefore, to prevent data corruption, all 3 bytes of the data register should be read subsequently using the register address pointer auto-increment feature of the serial interface.

To prevent losing some of the results, the VT DATA register should be read before the next conversion on the voltage / temperature channel is finished.

For voltage input, code 0 represents negative full scale ($-V_{REF}$), code 0x800000 represents zero scale (0 V) and the code 0xFFFFFF represents positive full scale ($+V_{REF}$).

To prevent losing some of the results, the VT DATA register should be read before the next conversion on the voltage /temperature channel is finished.

For temperature sensor, the temperature can be calculated from code using equation:

Temperature (°C) = (Code / 2048) - 4096

CAP SETUP REGISTER

Address pointer 0x07, default value 0x00

Capacitive channel setup.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	CAPEN	-	DIFF	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Description
7	CAPEN	CAPEN = 1 enables capacitive channel for single conversion, continuous conversion or calibration.
6	-	This bit must be 0 for proper operation.
5	DIFF	DIFF = 1 sets differential mode on the selected capacitive input.
4-0	-	These bits must be 0 for proper operation.

VT SETUP REGISTER

Address pointer 0x08, default value 0x00

Voltage / Temperature channel setup.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	VTEN	VTMD1	VTMD0	EXTREF	-	-	VTSHORT	VTCHOP
Default	0	0	0	0	0	0	0	0

<table>
<tr><th>Bit</th><th>Mnemonic</th><th>Description</th></tr>
<tr><td>7</td><td>VTEN</td><td>VTEN = 1 enables voltage / temperature channel for single conversion, continuous conversion or calibration.</td></tr>
<tr><td>6
5</td><td>VTMD1
VTMD0</td><td>Voltage / temperature channel input configuration:
<table>
<tr><th>VTMD1</th><th>VTMD0</th><th>Channel Input</th></tr>
<tr><td>0</td><td>0</td><td>Internal Temperature Sensor</td></tr>
<tr><td>0</td><td>1</td><td>External Temperature Sensor Diode</td></tr>
<tr><td>1</td><td>0</td><td>V_{DD} Monitor</td></tr>
<tr><td>1</td><td>1</td><td>External Voltage Input (VIN)</td></tr>
</table></td></tr>
<tr><td>4</td><td>EXTREF</td><td>EXTREF = 1 selects an external reference voltage connected to REFIN(+), REFIN(–) for the voltage input or the V_{DD} Monitor.
EXTREF = 0 selects the on-chip internal reference. The internal reference must be used with the internal temperature sensor for proper operation.</td></tr>
<tr><td>3-2</td><td>-</td><td>These bits must be 0 for proper operation.</td></tr>
<tr><td>1</td><td>VTSHORT</td><td>VTSHORT = 1 internally shorts the voltage / temperature channel input.</td></tr>
<tr><td>0</td><td>VTCHOP = 1</td><td>VTCHOP = 1 sets internal chopping on the voltage / temperature channel.
The VTCHOP bit must be set to 1 for the specified voltage / temperature channel performance.</td></tr>
</table>

EXC SETUP REGISTER

Address pointer 0x09, default value 0x03

Capacitive channel excitation setup.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	CLKCTRL	-	-	-	-	-	EXCLVL1	EXCLVL0
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Description
7	CLKCTRL	The CLKCTRL must be set 0 for proper capacitive channel operation. CLKCTRL = 1 increases the excitation signal frequency and the modulator clock frequency by factor of 2. This also decreases the conversion time on all channels (capacitive, voltage and temperature) by factor of 2.
6-2	-	These bits must be 0 for proper operation.
1 0	EXCLVL1, EXCLVL0	Excitation Voltage Level:

EXCLVL1	EXCLVL0	Voltage on Cap.	EXC pin Low Level	EXC pin High Level
0	0	$\pm V_{DD}/8$	$V_{DD} \times 3/8$	$V_{DD} \times 5/8$
0	1	$\pm V_{DD}/4$	$V_{DD} \times 1/4$	$V_{DD} \times 3/4$
1	0	$\pm V_{DD} \times 3/8$	$V_{DD} \times 1/8$	$V_{DD} \times 7/8$
1	1	$\pm V_{DD}/2$	0	V_{DD}

CONFIGURATION REGISTER

Address pointer 0x0A, default value 0xA0

Converter update rate and mode of operation setup.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	VTF1	VTF0	CAPF2	CAPF1	CAPF0	MD2	MD1	MD0
Default	0	0	0	0	0	0	0	0

Bit 7, Bit 6 — Mnemonic: VTF1, VTF0

Voltage / temperature channel digital filter setup - conversion time / update rate setup.
The conversion times in this table are valid for the CLKCTRL = 0 in the EXC SETUP register.
The conversion times are shorter by factor of two for the CLKCTRL = 1.

		VTCHOP = 1	
VTF1	VTF0	Conversion Time (ms)	Update Rate (Hz)
0	0	40.2	24.9
0	1	64.2	15.6
1	0	124.2	8.1
1	1	244.2	4.1

Bit 5, Bit 4, Bit 3 — Mnemonic: CAPF2, CAPF1, CAPF0

Capacitive channel digital filter setup - conversion time / update rate setup.
The conversion times in this table are valid for the CLKCTRL = 0 in the EXC SETUP register.
The CLKCTRL must be set 0 for proper capacitive channel operation.

CAPF2	CAPF1	CAPF0	Conversion Time (ms)	Update Rate (Hz)
0	0	0	22.0	45.5
0	0	1	23.8	41.9
0	1	0	40.0	25.0
0	1	1	76.0	13.2
1	0	0	124.0	8.1
1	0	1	154.0	6.5
1	1	0	184.0	5.5
1	1	1	219.2	4.6

Bit 2, Bit 1, Bit 0 — Mnemonic: MD2, MD1, MD0

Converter mode of operation setup

MD2	MD1	MD0	Mode
0	0	0	Idle
0	0	1	Continuous Conversion
0	1	0	Single Conversion
0	1	1	Power-Down
1	0	0	-
1	0	1	Capacitance Offset Calibration
1	1	0	Capacitance or Voltage Gain Calibration
1	1	1	

CAP DAC A REGISTER

Address pointer 0x0B, default value 0x00

Capacitive DAC setup.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	DACAENA	-	DACA – 6-Bit Value					
Default	0	0	0x00					

Bit	Mnemonic	Description
7	DACAENA	DACAENA = 1 connects capacitive DAC A to the positive capacitance input.
6	-	This bit must be 0 for proper operation.
6-1	DACA	DAC A value, code 0x00 ≈ 0pF, code 0x3F ≈ Full Range

CAP DAC B REGISTER

Address pointer 0x0C, default value 0x00

Capacitive DAC setup.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	DACAENB	-	DACA – 6-Bit Value					
Default	0	0	0x00					

Bit	Mnemonic	Description
7	DACBEN	DACBENB = 1 connects capacitive DAC B to the positive capacitance input.
		This bit must be 0 for proper operation.
6-1	DACB	DAC B value, code 0x00 ≈ 0pF, code 0x3F ≈ Full Range

CAP OFFSET REGISTER

16 bits, address pointer 0x0D, 0x0E default value 0x8000

Capacitive offset calibration register. The register holds capacitive channel zero-scale calibration coefficient. The value in this register is used to digitally remove the capacitive channel offset. The value in this register is updated automatically following the execution of a capacitance offset calibration. The capacitive offset calibration resolution (cap offset register LSB) is less than 64 aF, the full range is 2 pF.

CAP GAIN REGISTER

16 bits, address pointer 0x0F, 0x10, default value 0xXXXX

Capacitive gain calibration register. The register holds capacitive channel full scale factory calibration coefficient.

VOLT GAIN REGISTER

16 bits, address pointer 0x11,0x12, default value 0xXXXX

Voltage gain calibration register. The register holds voltage channel full scale factory calibration coefficient.

TYPICAL APPLICATION DIAGRAM

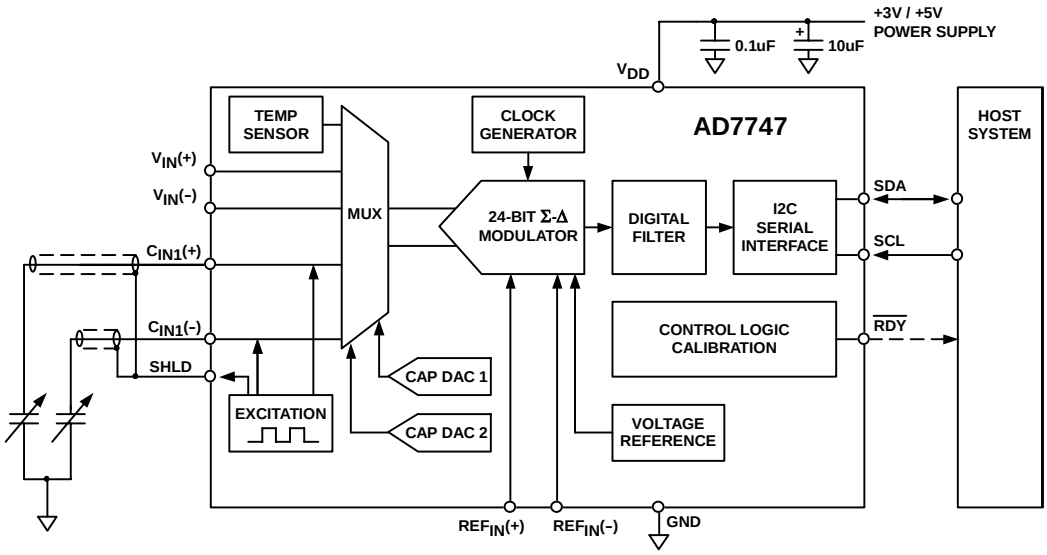

Figure 6. Basic Application Diagram for a Differential Capacitive Sensor

OUTLINE DIMENSIONS

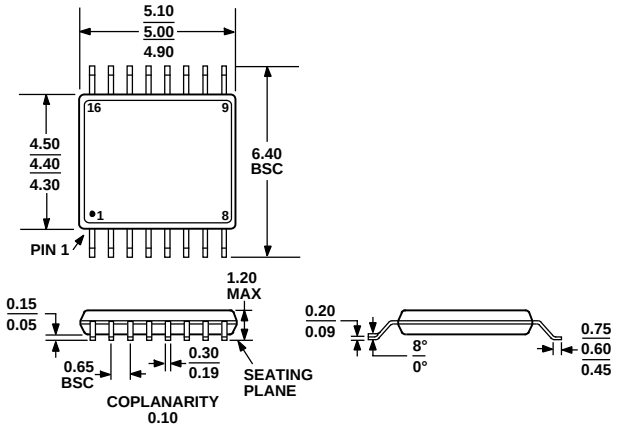

Figure 7. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)
Dimensions shown in millimeters

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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