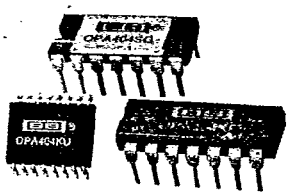
BURR-BROWN®



# OPA404

MILITARY & DIE VERSIONS AVAILABLE

## Quad High-Speed Precision *Difet*® OPERATIONAL AMPLIFIER

### FEATURES

- WIDE BANDWIDTH: 6.4MHz
- HIGH SLEW RATE: 35V/μs
- LOW OFFSET: ±750μV max
- LOW BIAS CURRENT: ±4pA max
- FAST SETTLING: 1.5μs to 0.01%
- STANDARD QUAD PINOUT

### APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DETECTOR ARRAYS

### DESCRIPTION

The OPA404 is a high performance monolithic *Difet*® (dielectrically-isolated FET) quad operational amplifier. It offers an unusual combination of very-low bias current together with wide bandwidth and fast slew rate.

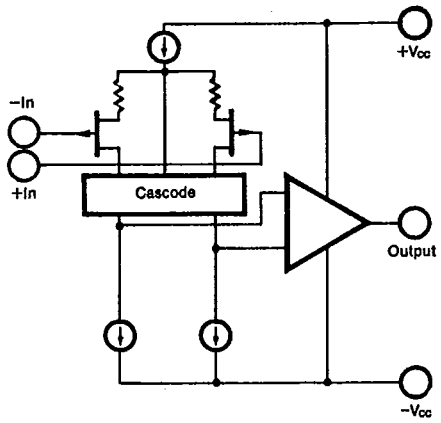
Noise, bias current, voltage offset, drift, and speed are superior to BIFET® amplifiers.

Laser trimming of thin-film resistors gives very-low offset and drift—the best available in a quad FET op amp.

The OPA404's input cascode design allows high precision input specifications and uncompromised high-speed performance.

Standard quad op amp pin configuration allows upgrading of existing designs to higher performance levels. The OPA404 is unity-gain stable.

*Difet*® Burr-Brown Corp., BIFET® National Semiconductor Corp.




OPA404 Simplified Circuit
(Each Amplifier)

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-677B

# SPECIFICATIONS

## ELECTRICAL

At $V_{CC} = \pm 15$VDC and $T_A = +25°C$ unless otherwise noted.

| PARAMETER | CONDITIONS | OPA404AG, KP, KU MIN | OPA404AG, KP, KU TYP | OPA404AG, KP, KU MAX | OPA404BG MIN | OPA404BG TYP | OPA404BG MAX | OPA404SG MIN | OPA404SG TYP | OPA404SG MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | | | | | |
| **NOISE**[1] | | | | | | | | | | | |
| Voltage: $f_O = 10$Hz | | | 32 | | | * | | | * | | nV/√Hz |
| $f_O = 100$Hz | | | 19 | | | * | | | * | | nV/√Hz |
| $f_O = 1$kHz | | | 15 | | | * | | | * | | nV/√Hz |
| $f_O = 10$kHz | | | 12 | | | * | | | * | | nV/√Hz |
| $f_B = 10$Hz to 10kHz | | | 1.4 | | | * | | | * | | μV, rms |
| $f_B = 0.1$Hz to 10Hz | | | 0.95 | | | * | | | * | | μV, p-p |
| Current: $f_B = 0.1$Hz to 10Hz | | | 12 | | | * | | | * | | fA, p-p |
| $f_O = 0.1$Hz to 20kHz | | | 0.6 | | | * | | | * | | fA/√Hz |
| **OFFSET VOLTAGE** | | | | | | | | | | | |
| Input Offset Voltage | $V_{CM} = 0$VDC | | ±260 | ±1mV | | * | ±750 | | * | * | μV |
| KP, KU | | | ±750 | ±2.5mV | | | | | | | μV |
| Average Drift | $T_A = T_{MIN}$ to $T_{MAX}$ | | ±3 | | | * | | | * | | μV/°C |
| KP | | | ±5 | | | | | | | | μV/°C |
| Supply Rejection | $\pm V_{CC} = 12$V to 18V | 80 | 100 | | 86 | * | | * | * | | dB |
| KP, KU | | 76 | 100 | | | | | | | | dB |
| Channel Separation | 100Hz, $R_L = 2$kΩ | | 125 | | | * | | | * | | dB |
| **BIAS CURRENT** | | | | | | | | | | | |
| Input Bias Current | $V_{CM} = 0$VDC | | ±1 | ±8 | | * | ±4 | | * | * | pA |
| KP, KU | | | ±1 | ±12 | | | | | | | pA |
| **OFFSET CURRENT** | | | | | | | | | | | |
| Input Offset Current | $V_{CM} = 0$VDC | | 0.5 | 8 | | * | 4 | | * | * | pA |
| KP, KU | | | 0.5 | 12 | | | | | | | pA |
| **IMPEDANCE** | | | | | | | | | | | |
| Differential | | | $10^{13} \| 1$ | | | * | | | * | | Ω \| pF |
| Common-Mode | | | $10^{14} \| 3$ | | | * | | | * | | Ω \| pF |
| **VOLTAGE RANGE** | | | | | | | | | | | |
| Common-Mode Input Range | | ±10.5 | +13, −11 | | * | * | | * | * | | V |
| Common-Mode Rejection | $V_{IN} = \pm 10$VDC | 88 | 100 | | 92 | * | | * | * | | dB |
| KP, KU | | 84 | 100 | | | | | | | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | | | | | | | |
| Open-Loop Voltage Gain | $R_L \geq 2$kΩ | 88 | 100 | | 92 | * | | * | * | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | | | | |
| Gain Bandwidth | Gain = 100 | 4 | 6.4 | | 5 | * | | * | * | | MHz |
| Full Power Response | 20V p-p, $R_L = 2$kΩ | | 570 | | | * | | | * | | kHz |
| Slew Rate | $V_O = \pm 10$V, $R_L = 2$kΩ | 24 | 35 | | 28 | * | | * | * | | V/μs |
| Settling Time: 0.1% | Gain = −1, $R_L = 2$kΩ | | 0.6 | | | * | | | * | | μs |
| 0.01% | $C_L = 100$pF, 10V step | | 1.5 | | | * | | | * | | μs |
| **RATED OUTPUT** | | | | | | | | | | | |
| Voltage Output | $R_L = 2$kΩ | ±11.5 | +13.2, −13.8 | | * | * | | * | * | | V |
| Current Output | $V_O = \pm 10$VDC | ±5 | ±10 | | * | * | | * | * | | mA |
| Output Resistance | 1MHz, open loop | | 80 | | | * | | | * | | Ω |
| Load Capacitance Stability | Gain = +1 | | 1000 | | | * | | | * | | pF |
| Short Circuit Current | | ±10 | ±18 | ±20 | * | * | * | * | * | * | mA |
| **POWER SUPPLY** | | | | | | | | | | | |
| Rated Voltage | | | ±15 | | | * | | | * | | VDC |
| Voltage Range, Derated Performance | | ±5 | | ±18 | * | | * | * | | * | VDC |
| Current, Quiescent | $I_O = 0$mADC | | 9 | 10 | | * | * | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification | Ambient temp. | −25 | | +85 | * | | * | −55 | | +125 | °C |
| KP, KU | | 0 | | +70 | | | | | | | °C |
| Operating | Ambient temp. | −55 | | +125 | * | | * | * | | * | °C |
| KP, KU | | −25 | | +85 | | | | | | | °C |
| Storage | Ambient temp. | −65 | | +150 | * | | * | * | | * | °C |
| θ Junction-Ambient | | | 100 | | | * | | | * | | °C/W |
| KP, KU | | | 120/100 | | | | | | | | °C/W |

*Specification same as OPA404AG.

NOTES: (1) Noise testing available—inquire.

## ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC}$ = ±15VDC and $T_A = T_{MIN}$ to $T_{MAX}$ unless otherwise noted.

| PARAMETER | CONDITIONS | OPA404AG, KP, KU MIN | OPA404AG, KP, KU TYP | OPA404AG, KP, KU MAX | OPA404BG MIN | OPA404BG TYP | OPA404BG MAX | OPA404SG MIN | OPA404SG TYP | OPA404SG MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification Range | Ambient temp. | –25 | | +85 | * | | * | –55 | | +125 | °C |
| KP, KU | | 0 | | +70 | | | | | | | °C |
| **INPUT** | | | | | | | | | | | |
| **OFFSET VOLTAGE** | | | | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0VDC | | ±450 | 2mV | | * | ±1.5mV | | ±550 | ±2.5mV | µV |
| KP, KU | | | ±1 | ±3.5 | | | | | | | mV |
| Average Drift | | | ±3 | | | * | | | * | | µV/°C |
| KP, KU | | | ±5 | | | | | | | | µV/°C |
| Supply Rejection | | 75 | 96 | | 80 | * | | 70 | 93 | | dB |
| **BIAS CURRENT** | | | | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC | | ±32 | ±200 | | * | ±100 | | ±500 | ±5nA | pA |
| **OFFSET CURRENT** | | | | | | | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC | | 17 | 100 | | * | 50 | | 260 | 2.5nA | pA |
| **VOLTAGE RANGE** | | | | | | | | | | | |
| Common-Mode Input Range | | ±10.2 | +12.7, –10.6 | | * | * | | ±10 | +12.6, –10.5 | | V |
| Common-Mode Rejection | $V_{IN}$ = ±10VDC | 82 | 99 | | 86 | * | | 80 | 88 | | dB |
| KP, KU | | 80 | 99 | | | | | | | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | | | | | | | |
| Open-Loop Voltage Gain | $R_L \geq 2k\Omega$ | 82 | 94 | | 86 | * | | 80 | 88 | | dB |
| **RATED OUTPUT** | | | | | | | | | | | |
| Voltage Output | $R_L$ = 2kΩ | ±11.5 | +12.9, –13.8 | | * | * | | ±11 | +12.7, –13.8 | | V |
| Current Output | $V_O$ = ±10VDC | ±5 | ±9 | | * | * | | * | ±8 | | mA |
| Short Circuit Current | $V_O$ = 0VDC | ±5 | ±12 | ±30 | * | * | * | ±8 | ±10 | * | mA |
| **POWER SUPPLY** | | | | | | | | | | | |
| Current, Quiescent | $I_O$ = 0mADC | | 9.3 | 10.5 | | * | * | | 9.4 | 11 | mA |

*Specification same as OPA404AG.

## ORDERING INFORMATION

OPA404 ( ) ( )

- Basic model number
- Performance grade
  - K = 0°C to +70°C
  - A, B = –25°C to +85°C
  - S = –55°C to +125°C
- Package code
  - G = 14-pin ceramic DIP
  - P = 14-pin plastic DIP
  - U = 16-Pin plastic SOIC

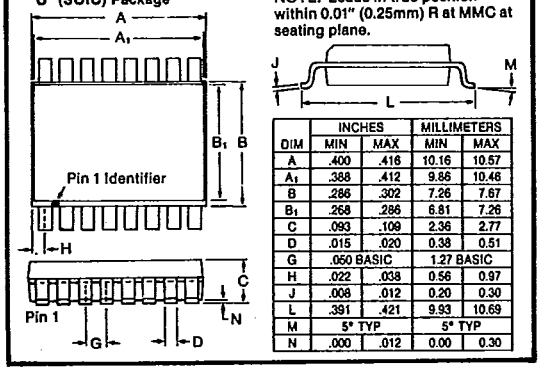
## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply | ±18VDC |
| Internal Power Dissipation[1] | 1000mW |
| Differential Input Voltage[2] | ±36VDC |
| Input Voltage Range[2] | ±18VDC |
| Storage Temperature Range | P, U = –40/+85°C, G = –65/+150°C |
| Operating Temperature Range | P, U = –25/+85°C, G = –55/+125°C |
| Lead Temperature (soldering, 10 seconds) | +300°C |
| Output Short Circuit Duration[3] | Continuous |
| Junction Temperature | +175°C |

NOTES:
(1) Packages must be derated based on $\theta_{JC}$ = 30°C/W or $\theta_{JA}$ = 120°C/W.
(2) For supply voltages less than ±18VDC the absolute maximum input voltage is equal to: 18V > $V_{IN}$ > $-V_{CC}$ – 8V. See Figure 2.
(3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and $T_J$.

## MECHANICAL

"U" (SOIC) Package




NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

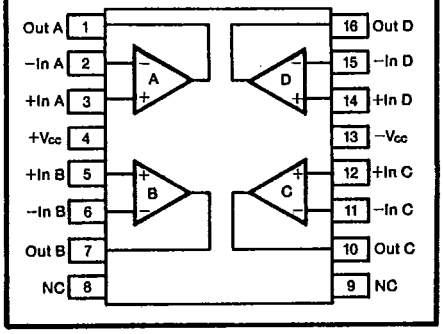



| DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|---|---|---|---|---|
| A | .400 | .416 | 10.16 | 10.57 |
| A1 | .388 | .412 | 9.86 | 10.46 |
| B | .286 | .302 | 7.26 | 7.67 |
| B1 | .268 | .286 | 6.81 | 7.26 |
| C | .093 | .109 | 2.36 | 2.77 |
| D | .015 | .020 | 0.38 | 0.51 |
| G | .050 BASIC | | 1.27 BASIC | |
| H | .022 | .038 | 0.56 | 0.97 |
| J | .008 | .012 | 0.20 | 0.30 |
| L | .391 | .421 | 9.93 | 10.69 |
| M | 5° TYP | | 5° TYP | |
| N | .000 | .012 | 0.00 | 0.30 |

## PIN CONFIGURATION

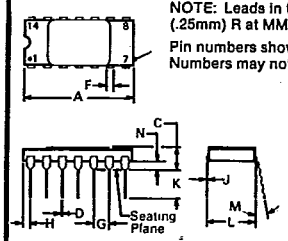
Top View

"U" (SOIC) Package



## MECHANICAL

**"G" Package**

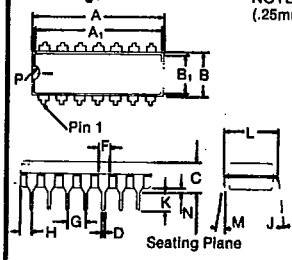


NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.
Pin numbers shown for reference only. Numbers may not be marked on package.

| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | .670 | .710 | 17.02 | 18.03 |
| C | .065 | .170 | 1.65 | 4.32 |
| D | .015 | .021 | 0.38 | 0.53 |
| F | .045 | .060 | 1.14 | 1.52 |
| G | .100 BASIC | | 2.54 BASIC | |
| H | .025 | .070 | 0.64 | 1.78 |
| J | .008 | .012 | 0.20 | 0.30 |
| K | .120 | .240 | 3.05 | 6.10 |
| L | .300 BASIC | | 7.62 BASIC | |
| M | — | 10° | — | 10° |
| N | .009 | .060 | 0.23 | 1.52 |

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

**"P" Package**



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

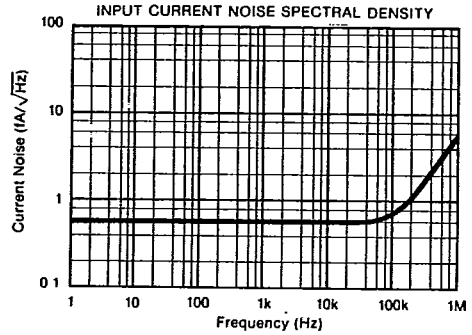
| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | .700 | .800 | 17.78 | 20.32 |
| $A_1$ | .685 | .785 | 17.40 | 19.94 |
| B | .230 | .290 | 5.85 | 7.38 |
| $B_1$ | .200 | .250 | 5.09 | 6.36 |
| C | .120 | .200 | 3.05 | 5.09 |
| D | .015 | .023 | 0.38 | 0.59 |
| F | .030 | .070 | 0.76 | 1.78 |
| G | .100 BASIC | | 2.54 BASIC | |
| H | .050 | .100 | 1.27 | 2.54 |
| J | .008 | .015 | 0.20 | 0.38 |
| K | .070 | .150 | 1.78 | 3.82 |
| L | .300 BASIC | | 7.63 BASIC | |
| M | 0° | 15° | 0° | 15° |
| N | .010 | .030 | 0.25 | 0.76 |
| P | .025 | .050 | 0.64 | 1.27 |

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

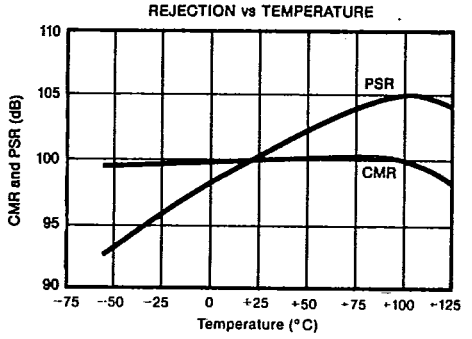
# TYPICAL PERFORMANCE CURVES

$T_A$ = +25°C, $V_{CC}$ = ±15VDC unless otherwise noted.

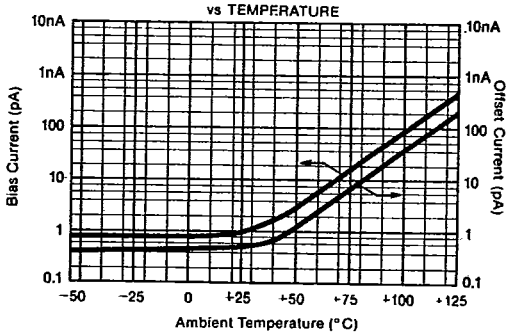
INPUT CURRENT NOISE SPECTRAL DENSITY




POWER SUPPLY REJECTION AND COMMON-MODE REJECTION vs TEMPERATURE

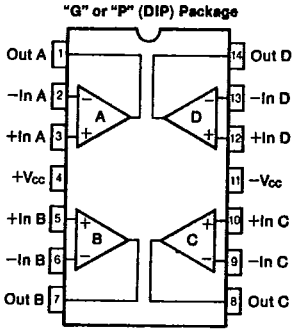



BIAS AND OFFSET CURRENT vs TEMPERATURE

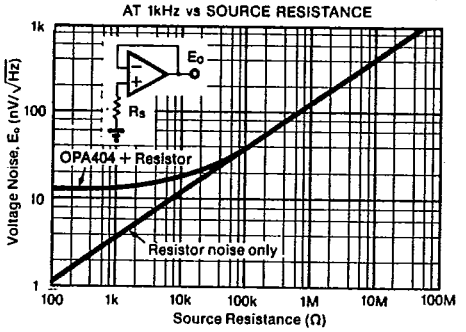



## CONNECTION DIAGRAM

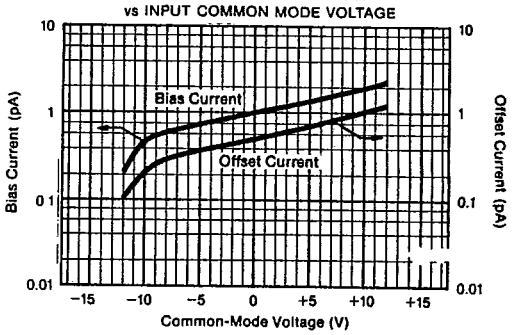
**Top View**[1] **"G" or "P" (DIP) Package**




TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



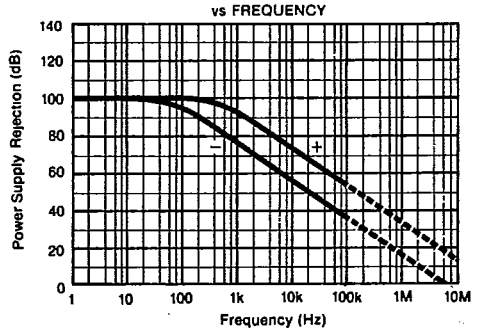

BIAS AND OFFSET CURRENT vs INPUT COMMON MODE VOLTAGE



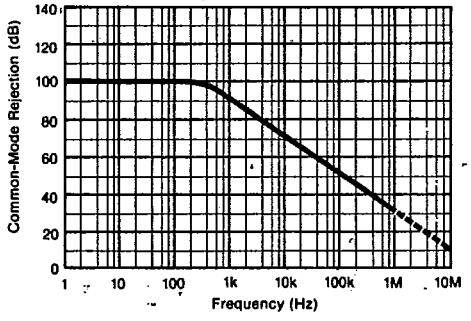
## TYPICAL PERFORMANCE CURVES [CONT]

$T_A$ = +25°C, $V_{CC}$ = ±15VDC unless otherwise noted.

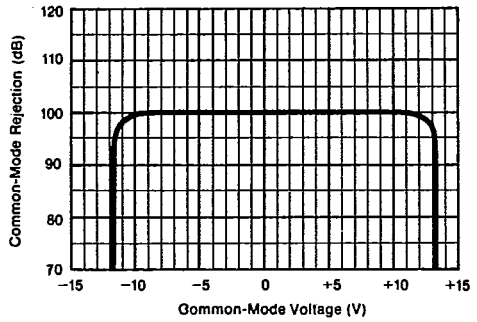
POWER SUPPLY REJECTION vs FREQUENCY



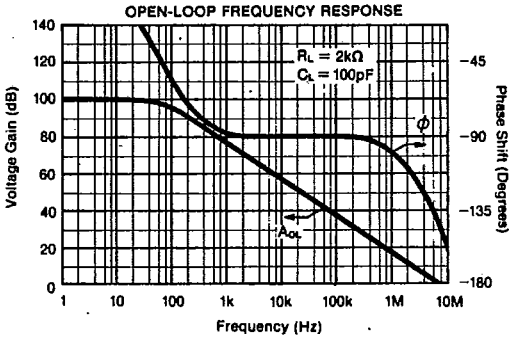

COMMON-MODE REJECTION vs FREQUENCY



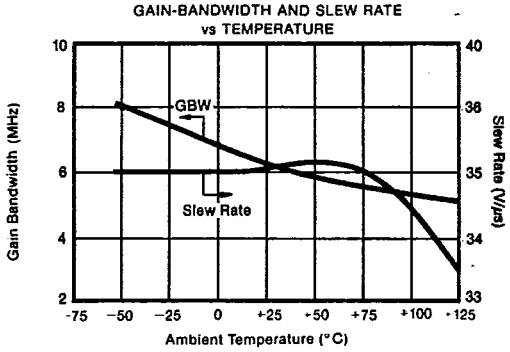

COMMON-MODE REJECTION vs INPUT COMMON MODE VOLTAGE



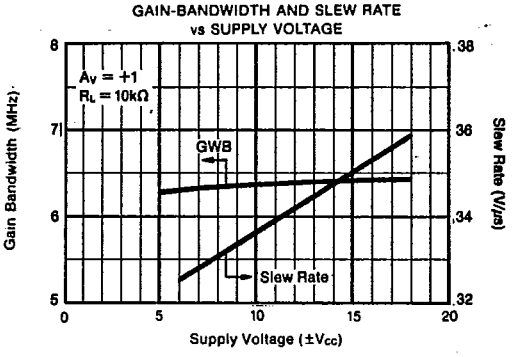

OPEN-LOOP FREQUENCY RESPONSE



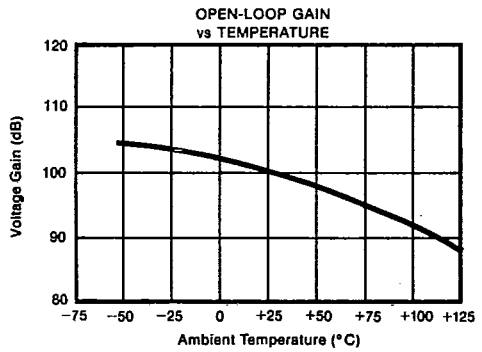

GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



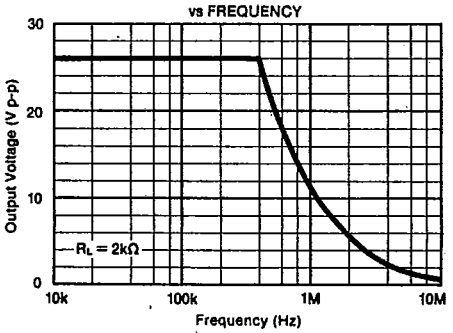

GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE




OPEN-LOOP GAIN vs TEMPERATURE



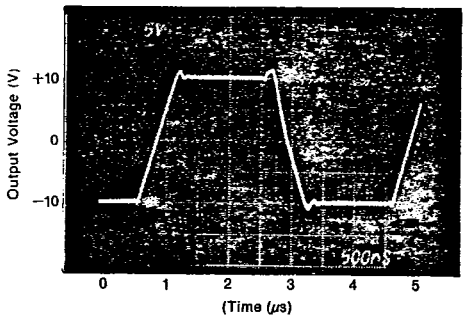

MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



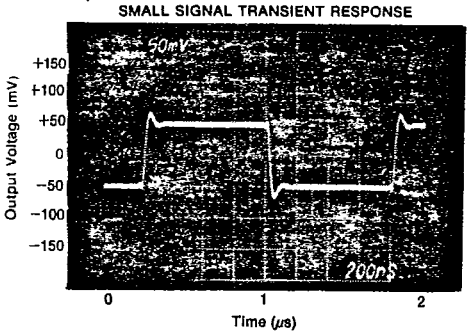
## TYPICAL PERFORMANCE CURVES [CONT]

$T_A$ = +25°C, $V_{CC}$ = ±15VDC unless otherwise noted.

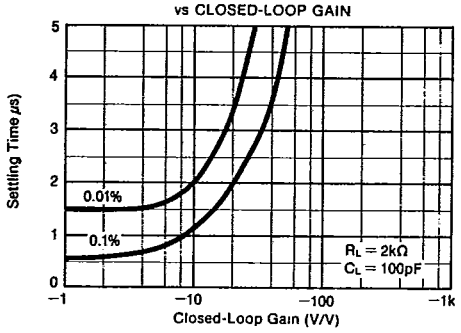
LARGE SIGNAL TRANSIENT RESPONSE



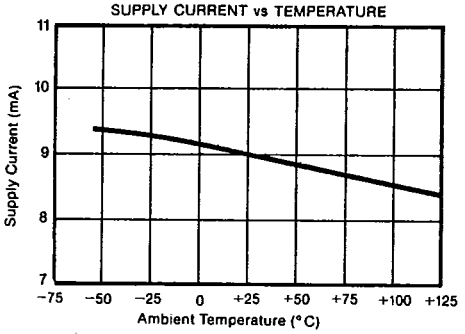

SMALL SIGNAL TRANSIENT RESPONSE



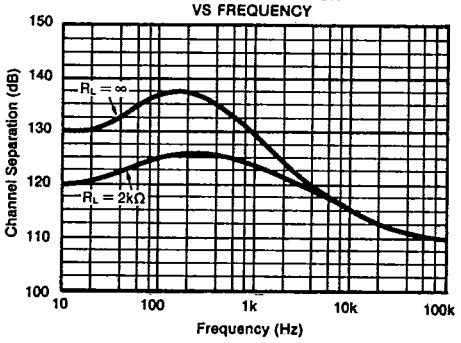

SETTLING TIME vs CLOSED-LOOP GAIN



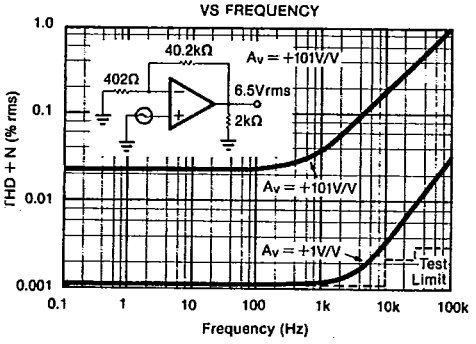

SUPPLY CURRENT vs TEMPERATURE



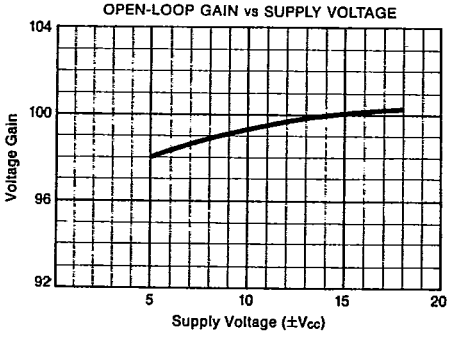

CHANNEL SEPARATION VS FREQUENCY



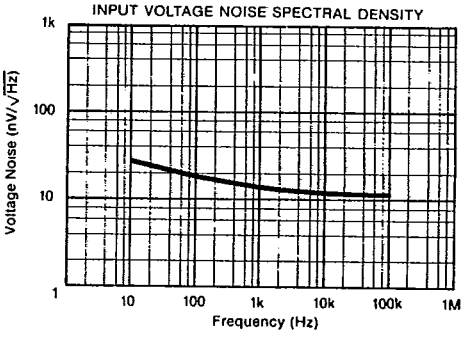

TOTAL HARMONIC DISTORTION VS FREQUENCY




OPEN-LOOP GAIN vs SUPPLY VOLTAGE




INPUT VOLTAGE NOISE SPECTRAL DENSITY



# APPLICATIONS INFORMATION

## OFFSET VOLTAGE ADJUSTMENT

The OPA404 offset voltage is laser-trimmed and will require no further trim for most applications. If desired, offset voltage can be trimmed by summing (see Figure 1). With this trim method there will be no degradation of input offset drift.

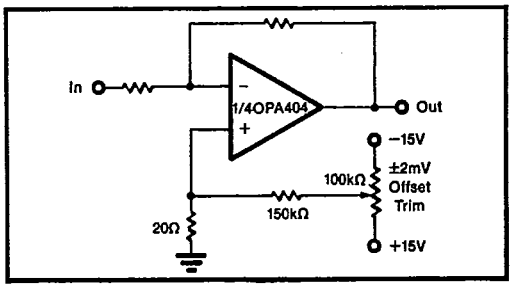



FIGURE 1. Offset Voltage Trim.

## INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET® amplifiers can be destroyed by the loss of $-V_{CC}$

Unlike BIFET® amplifiers, the *Difet*® OPA404 requires input current limiting resistors only if its input voltage can exceed −8V. A 10kΩ series resistor will limit the input current to a safe value with up to ±15V input levels even if both supply voltages are lost. (See Figure 2 and Absolute Maximum Ratings).

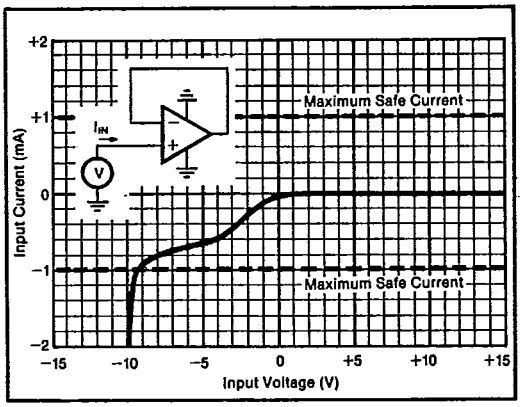



FIGURE 2. Input Current vs Input Voltage with $\pm V_{CC}$ Pins Grounded.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

## GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA404. To avoid leakage, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input ptotential (see Figure 3).

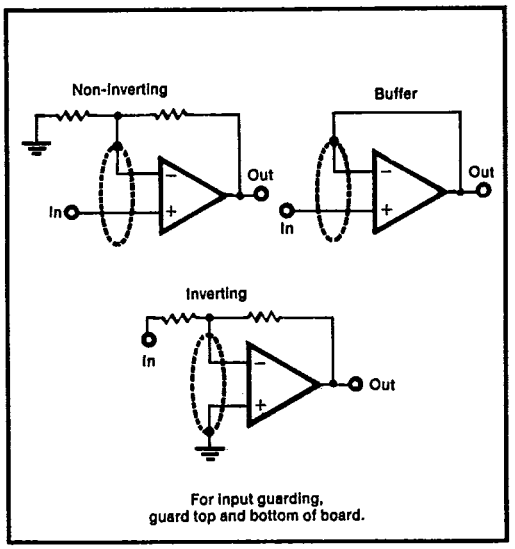



FIGURE 3. Connection of Input Guard.

## HANDLING AND TESTING

Measuring the unusually low bias current of the OPA404 is difficult without specialized test equipment; most commercial benchtop testers cannot accurately measure the OPA404 bias current. Low-leakage test sockets and special test fixtures are recommended if incoming inspection of bias current is to be performed.

To prevent surface leakage between pins, the DIP package should not be handled by bare fingers. Oils and salts from fingerprints or careless handling can create leakage currents that exceed the specified OPA404 bias currents.

If necessary, DIP packages and PC board assemblies can be cleaned with Freon TF®, baked for 30 minutes at 85°C, rinsed with de-ionized water, and baked again for 30 minutes at 85°C. Surface contamination can be prevented by the application of a high-quality conformal coating to the cleaned PC board assembly.

## BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET® operational amplifiers are affected by common-mode voltage (Figure 4). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely-low bias current of the OPA404 is not compromised by common-mode voltage.

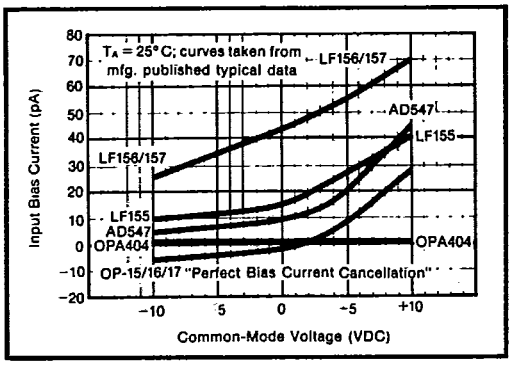



FIGURE 4. Input Bias Current Versus Common-Mode Voltage.

## APPLICATIONS CIRCUITS

Figures 5 through 11 are circuit diagrams of various applications for the OPA404.

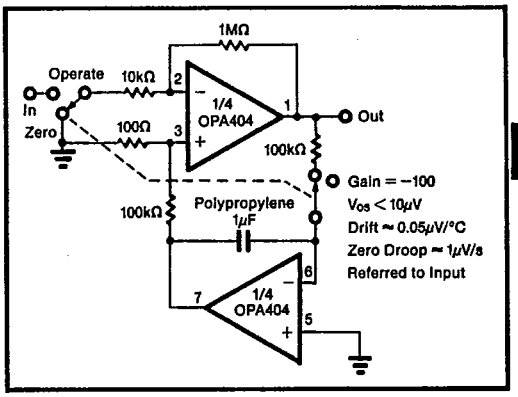



FIGURE 5. Auto-Zero Amplifier.

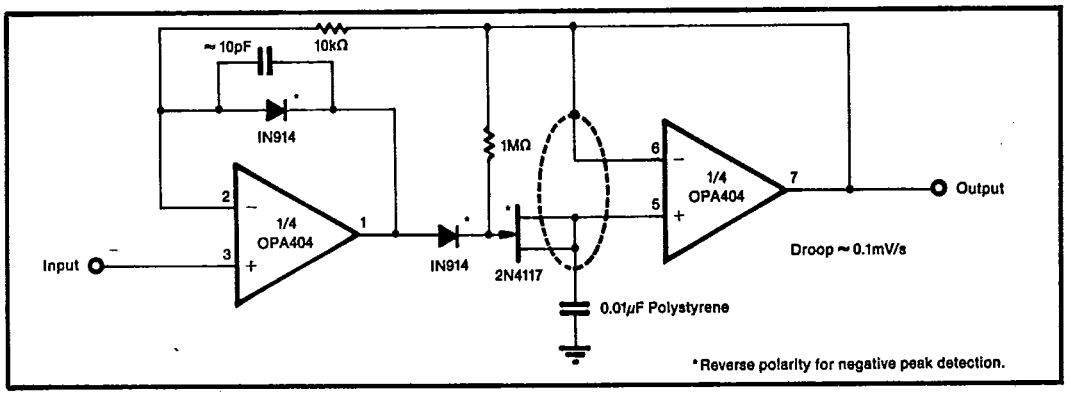



FIGURE 6. Low-Droop Positive Peak Detector.

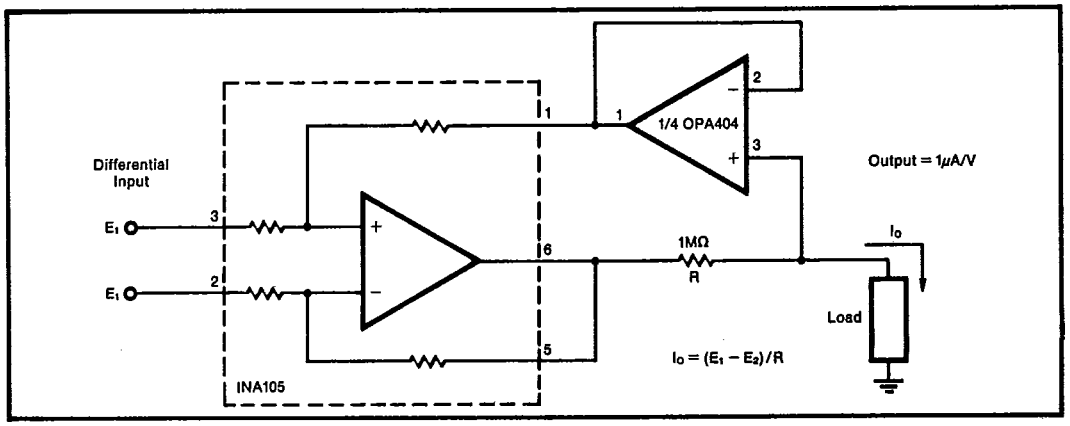



FIGURE 7. Voltage-Controlled Microamp Currrent Source.

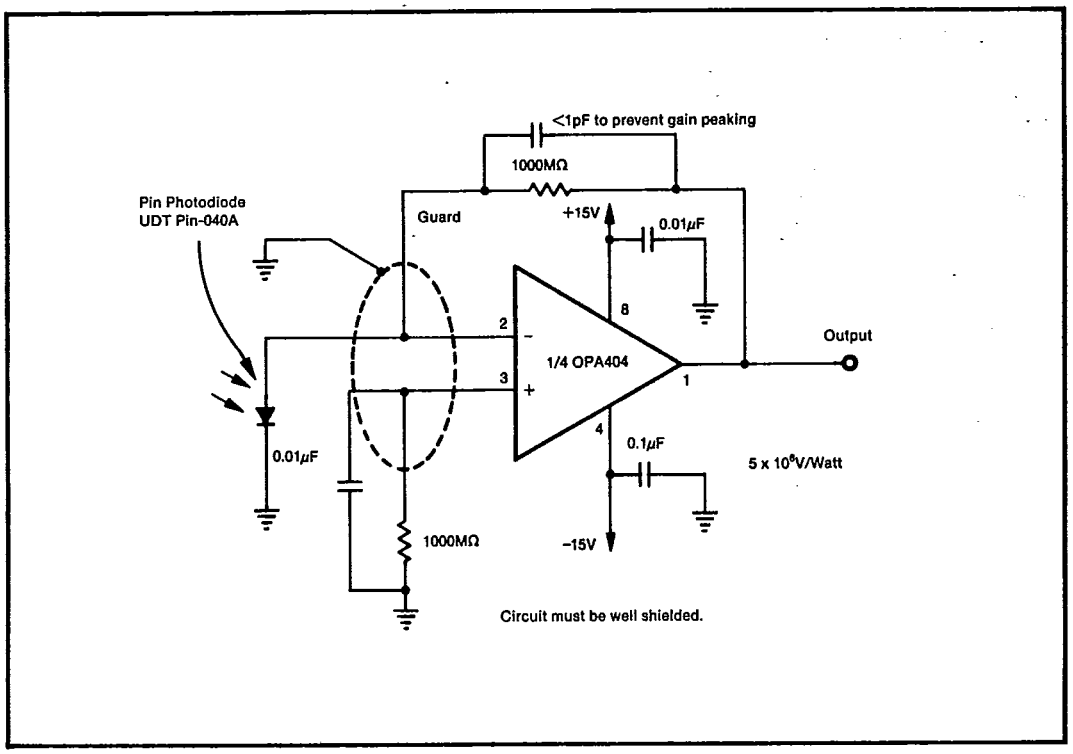



FIGURE 8. Sensitive Photodiode Amplifier.

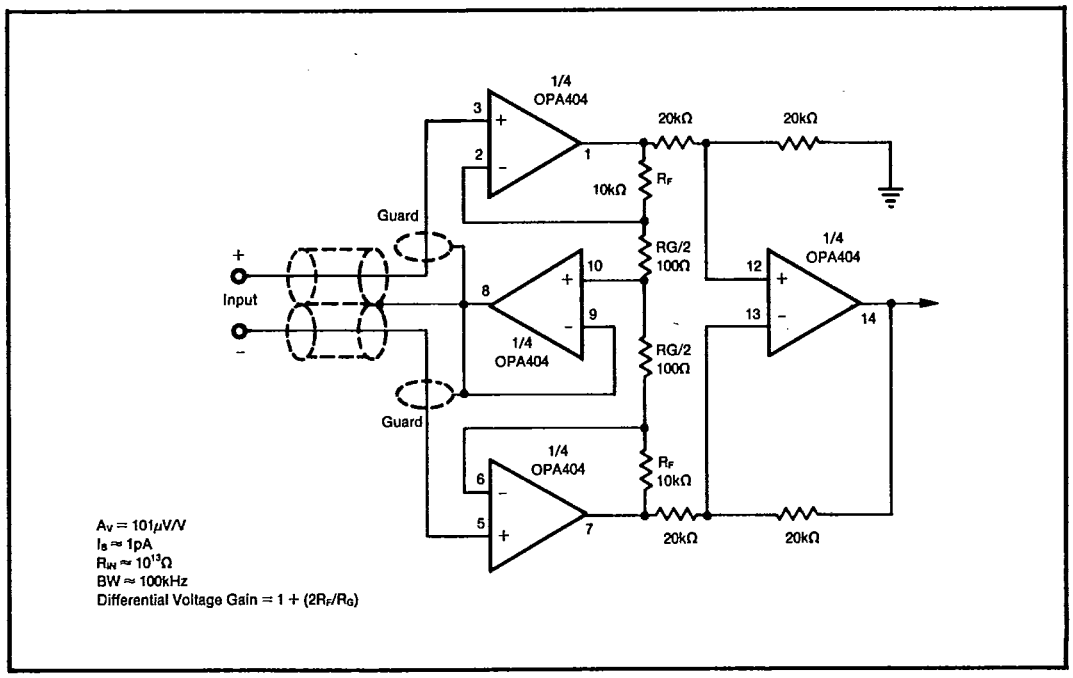



FIGURE 9. FET Instrumentation Amplifier with Shield Driver.

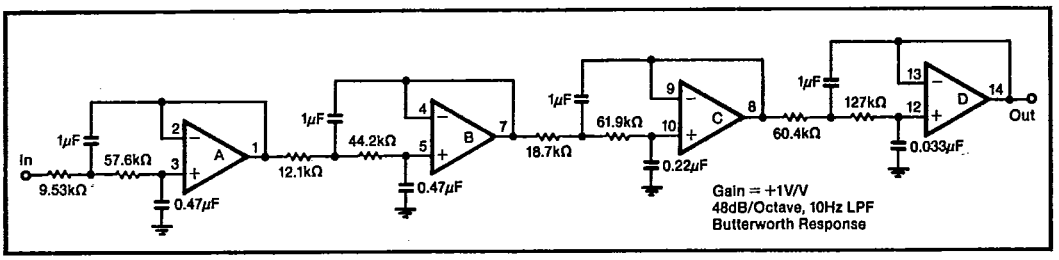



FIGURE 10. 8-Pole 10Hz Low-Pass Filter.

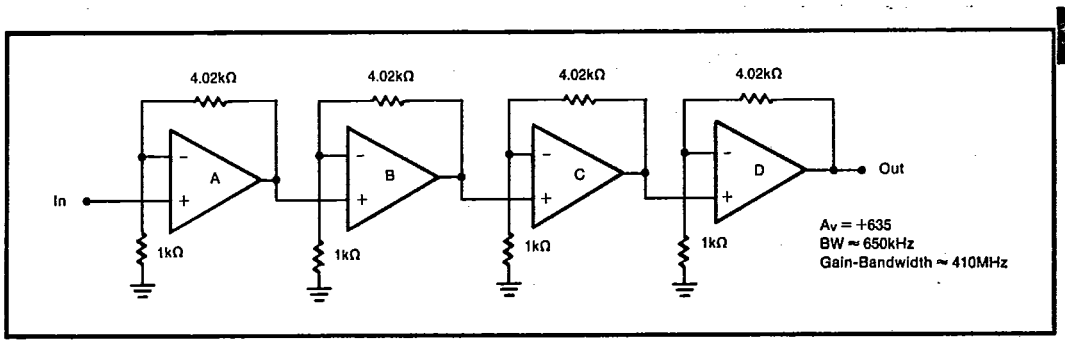



FIGURE 11. Wide-Band Amplifier