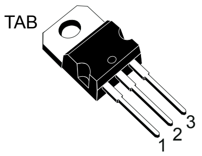
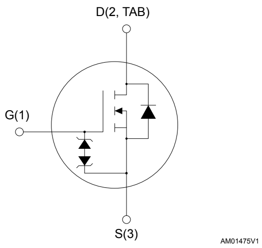
STP7N52DK3

Datasheet

N-channel 525 V, 0.95 Ω typ., 6 A, SuperFREDmesh3™ Power MOSFET in a TO-220 package



TO-220



Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STP7N52DK3	525 V	1.15 Ω	6 A	90 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

This device is developed using the revolutionary N-channel SuperFREDmesh3™ technology. It associates all advantages of reduced on-resistance, Zener gate protection and very high dv/dt capability with a fast body-drain recovery diode. Such series complements the FDmesh™ advanced technology.

Product status link
STP7N52DK3

Product summary	
Order code	STP7N52DK3
Marking	7N52DK3
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	525	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	6	A
	Drain current (continuous) at T_C = 100 °C	4	A
I_{DM} (1)	Drain current (pulsed)	24	A
P_{TOT}	Total dissipation at T_C = 25 °C	90	W
I_{AR} (2)	Avalanche current, repetitive or non-repetitive	3	A
E_{AS} (3)	Single pulse avalanche energy	110	mJ
dv/dt (4)	Peak diode recovery voltage slope	20	V/ns
di/dt (4)	Diode reverse recovery current slope	400	A/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *Pulse width is limited by T_{Jmax}.*
3. *Starting T_J = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V*
4. *$I_{SD} \leq 6$ A, $V_{DS(peak)} \leq V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$*

Table 2. **Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.39	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	°C/W

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	525			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 525 V			1	µA
		V_{GS} = 0 V, V_{DS} = 525 V, T_C = 125 °C(1)			50	µA
I_{GSS}	Gate body leakage current	V_{GS} = ±20 V, V_{DS} = 0 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 3 A		0.95	1.15	Ω

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	870	-	pF
C_{oss}	Output capacitance			70		
C_{rss}	Reverse transfer capacitance			13		
$C_{oss(tr)}$(1)	Time-related equivalent output capacitance	V_{DS} = 0 to 420 V, V_{GS} = 0 V	-	53	-	pF
$C_{oss(er)}$(2)	Energy-related equivalent output capacitance		-	74	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	3.5	-	Ω
Q_g	Total gate charge	V_{DD} = 420 V, I_D = 6 A, V_{GS} = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	33	-	nC
Q_{gs}	Gate-source charge			5		
Q_{gd}	Gate-drain charge			19		

1. *$C_{oss(tr)}$ is defined as the constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 420 V.*
2. *$C_{oss(er)}$. is defined as the constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 420 V.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 260 V, I_D = 3 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	12	-	ns
t_r	Rise time			12		
$t_{d(off)}$	Turn-off delay time			37		
t_f	Fall time			19		

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		6	A
I_{SDM} (1)	Source-drain current (pulsed)				24	
V_{SD} (2)	Forward on voltage	I_{SD} = 6 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 6 A, di/dt = 100 A/µs,	-	110		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V		0.44		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)		8		A
t_{rr}	Reverse recovery time	I_{SD} = 6 A, di/dt = 100 A/µs,	-	140		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_j = 150 °C		0.68		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)		10		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

Table 7. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ±1 mA, I_D = 0 A	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

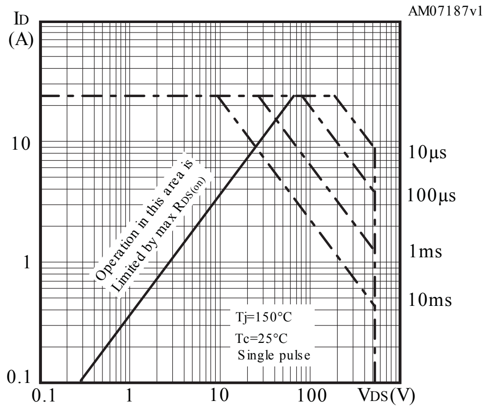


Figure 2. Thermal impedance

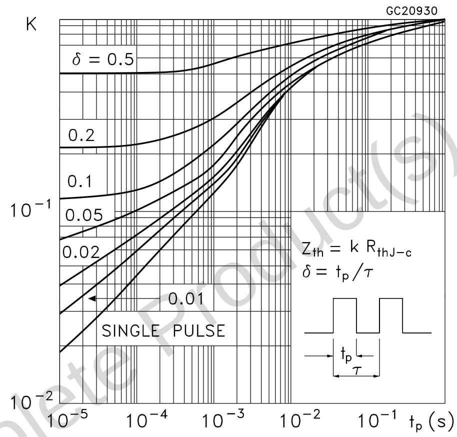


Figure 3. Output characteristics

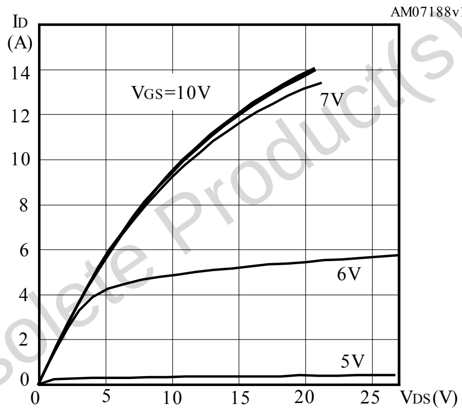


Figure 4. Transfer characteristics

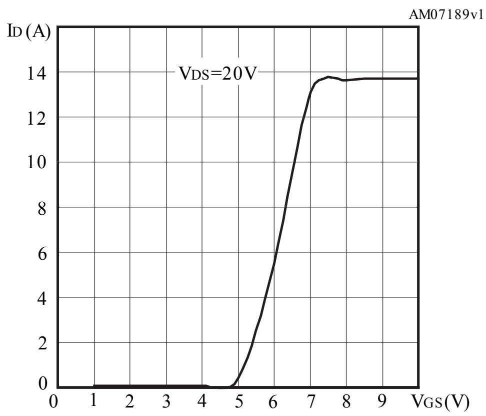


Figure 5. Gate charge vs gate-source voltage

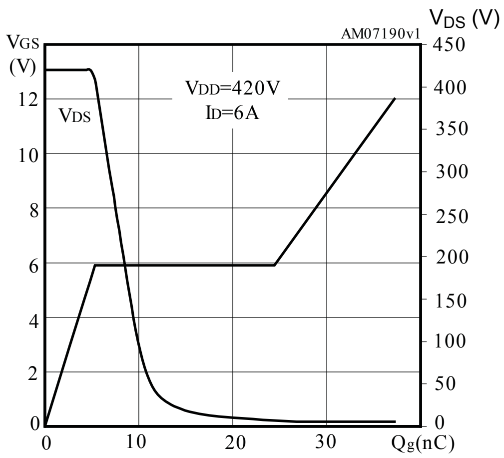


Figure 6. Static drain-source on-resistance

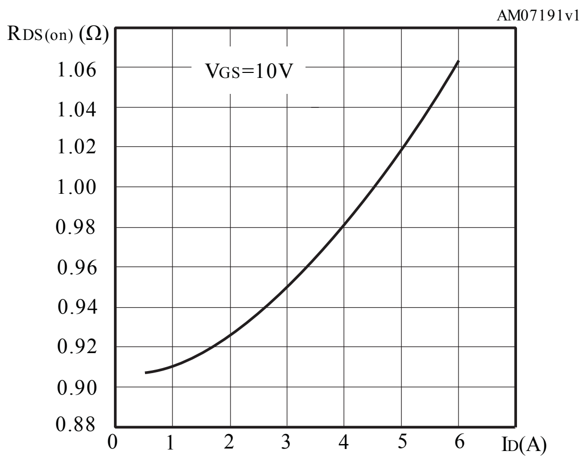


Figure 7. Capacitance variations

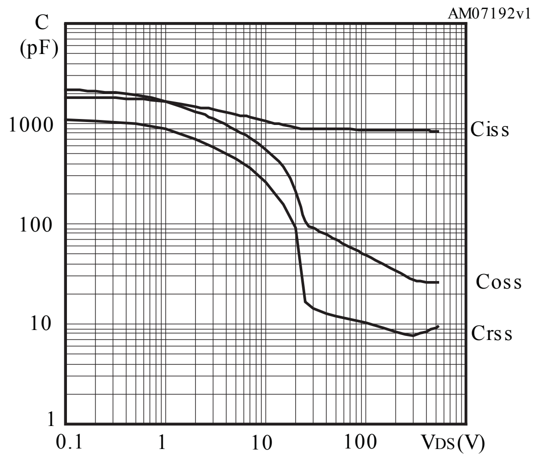


Figure 8. Output capacitance stored energy

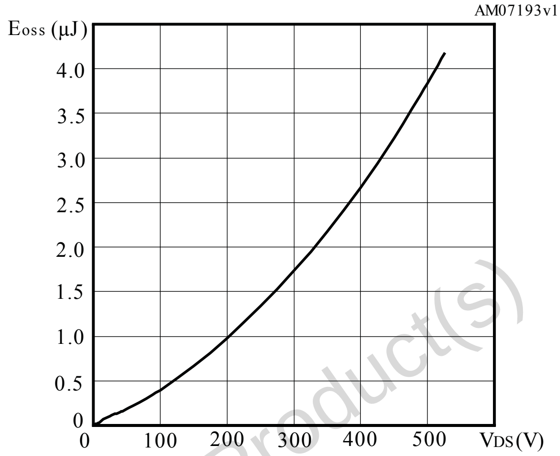


Figure 9. Normalized gate threshold voltage vs temperature

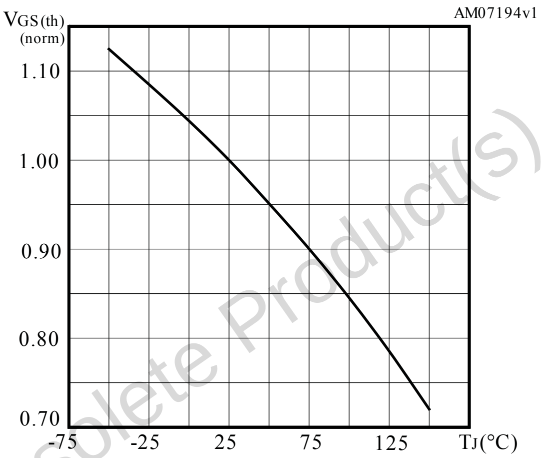


Figure 10. Normalized on-resistance vs temperature

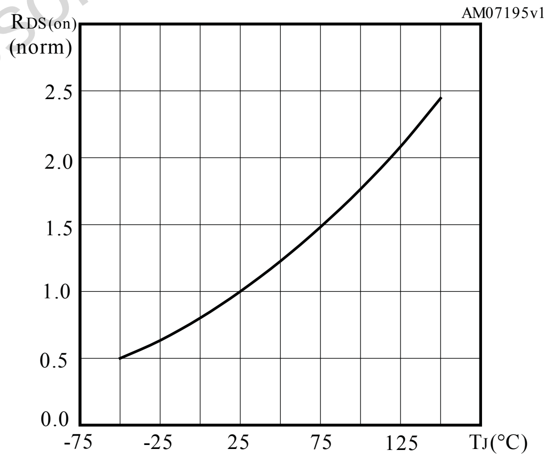


Figure 11. Source-drain diode forward characteristics

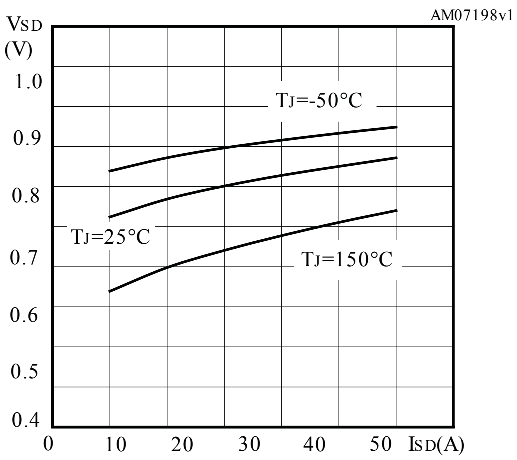


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature

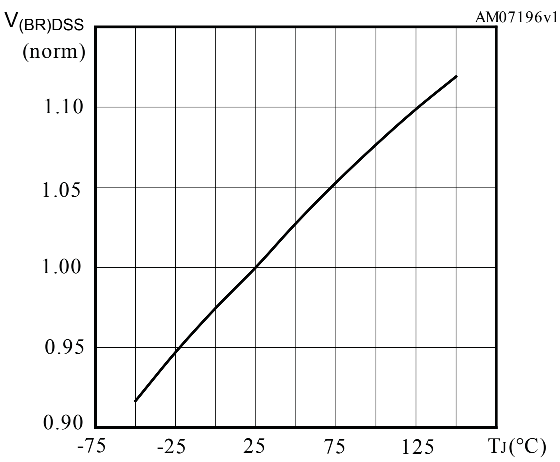
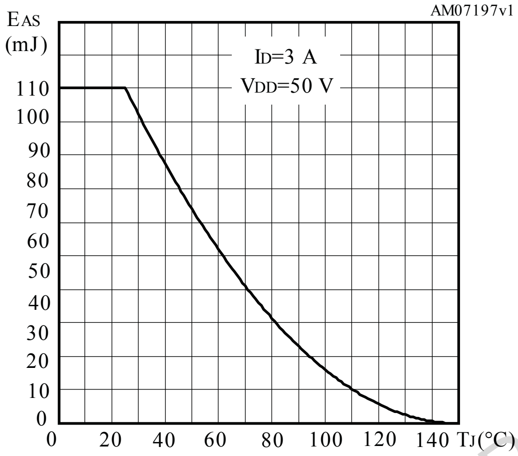


Figure 13. **Maximum avalanche energy vs starting T_J**



3 Test circuits

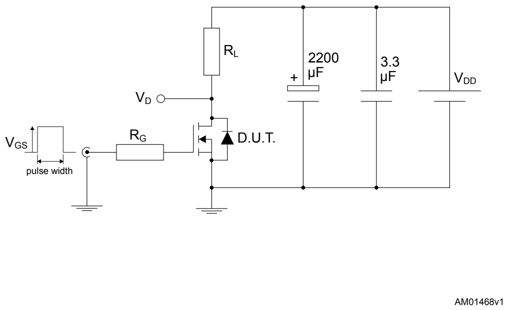


Figure 14. Test circuit for resistive load switching times

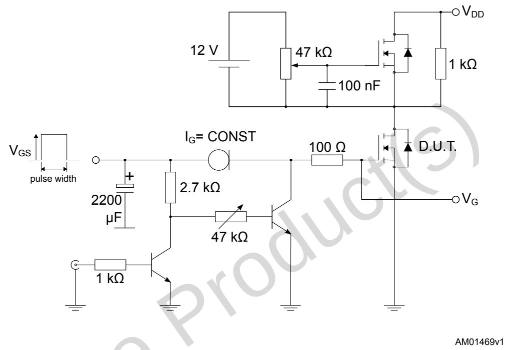


Figure 15. Test circuit for gate charge behavior

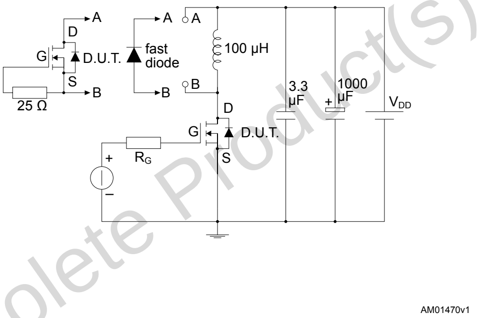


Figure 16. Test circuit for inductive load switching and diode recovery times

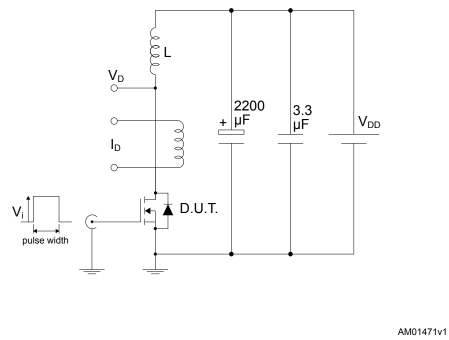


Figure 17. Unclamped inductive load test circuit

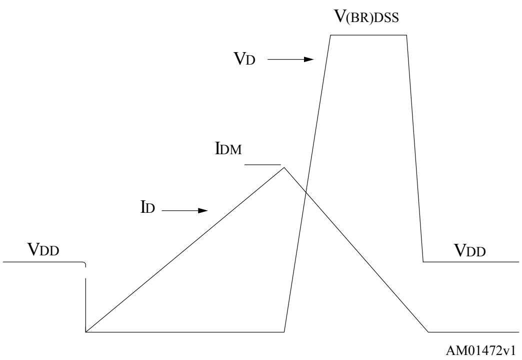


Figure 18. Unclamped inductive waveform

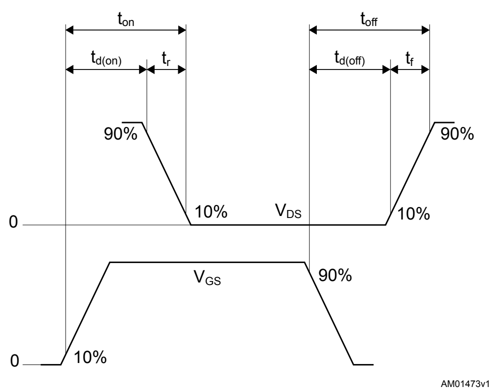


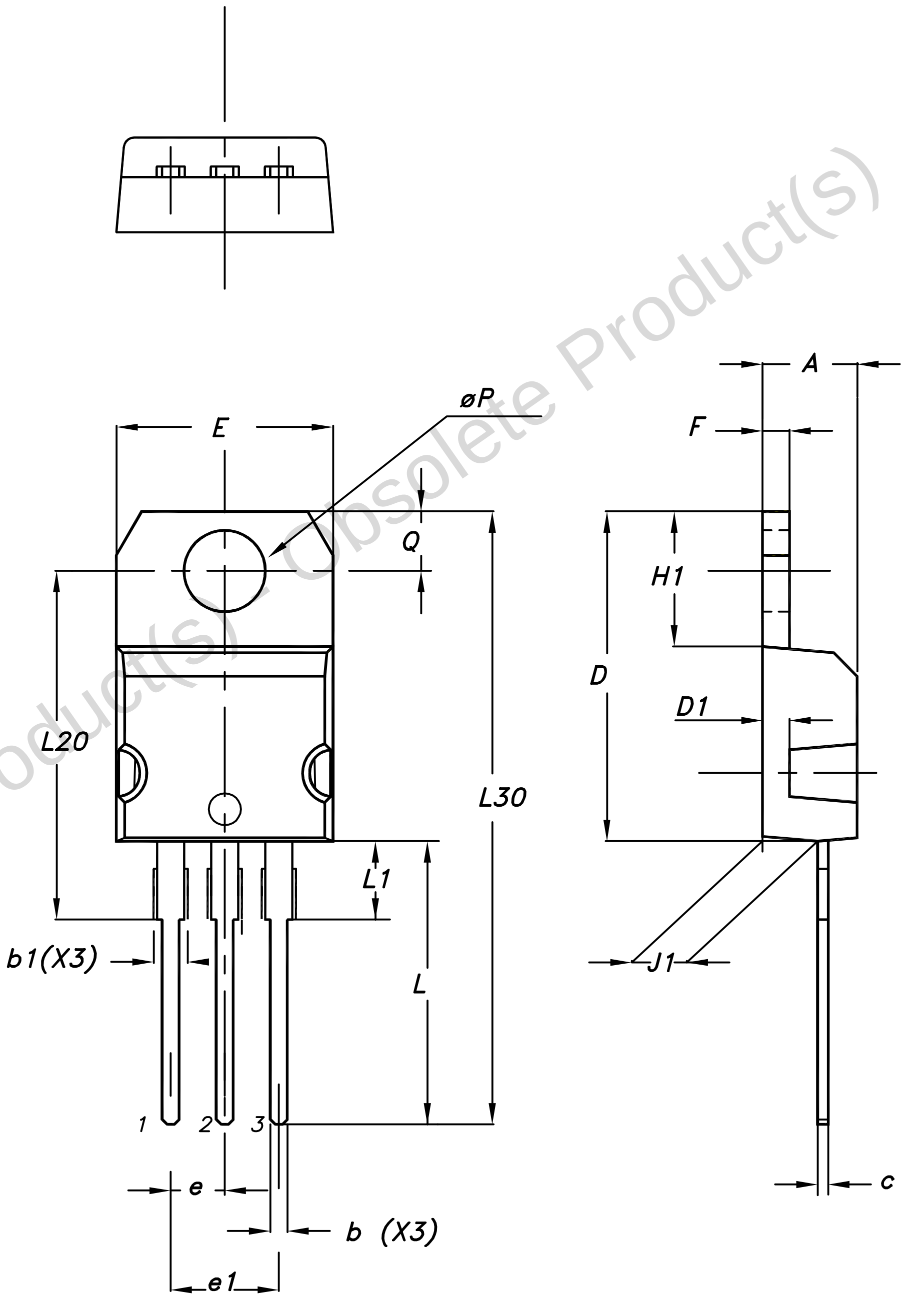
Figure 19. Switching time waveform

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220 type A package information

Figure 20. **TO-220 type A package outline**



0015988_typeA_Rev_21

Table 8. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

Revision history

Table 9. Document revision history

Date	Version	Changes
04-Oct-2018	1	Initial release. This part number was previously included in datasheet DS6515.

Contents