M21163

3.2 Gbps 32 Port Reconfigurable Non-Blocking Crosspoint Switch

The M21163 is a very low power, reconfigurable, 32 port, non-blocking digital crosspoint switch. The device is optimized for power and performance for data frequencies of up to 3.2 Gbps, including Serial Digital Interface (SDI) video data rates.

The M21163 is designed to provide the designer with the utmost choice and flexibility. With 24 reconfigurable input/output ports and 8 dedicated output ports, it may be used to create any square and non-square matrix size, from 24x8, to 16x16, to 1x31 and every size in between.

The M21163 includes signal conditioning to compensate for losses accumulated across long board traces, making it ideal for high-speed backplane switching applications. Each input/output port features individually programmable trace equalization when configured as an input, and individually programmable de-emphasis and output swing, when configured as an output. The dedicated output ports have individually programmable de-emphasis and swing control.

For lowest power consumption and ease of heat dissipation management, the device may be powered from a single 1.2 V supply. For ease of design and when DC coupling to a voltage other than 1.2 V is desired, the high-speed input and output ports, as well as the digital interface, may be powered from a 1.2 V, 1.8 V, 2.5 V or 3.3 V supply. Furthermore, the input/output ports include on-chip 50 Ω termination and are electrically isolated from one another, allowing each to be powered from and terminated to a different voltage rail. This provides additional flexibility as each port on the device may be DC coupled to upstream and downstream devices with different voltage rails.

The M21163 is offered in a green and RoHS compliant 17 mm x 17 mm, 252-pin, thermally enhanced BGA package.

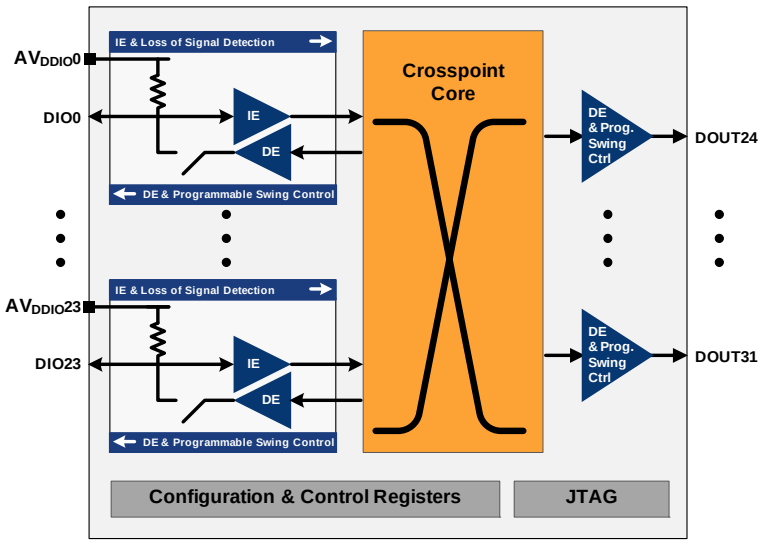
Features

- Reconfigurable IOs allowing for non-square matrix sizes
- Per port individually programmable input equalization and output de-emphasis
- Per port individually programmable output swing control
- Per port individual power down control
- Very low power operation (70 mW per channel @1.2 V typical)
- DC and AC coupling at the input and output with integrated level shifter
- Integrated 50 Ω input and output termination
- Loss of signal detection at the input
- Standard 2-wire and 4-wire serial digital interface
- Industrial operating temperature range of -40 °C to 85 °C

Applications

- Signal switching
- Fanout buffers
- Backplane equalizing and re-driving
- 3G/HD/SD-SDI switchers and routers

M21163 Device Architecture



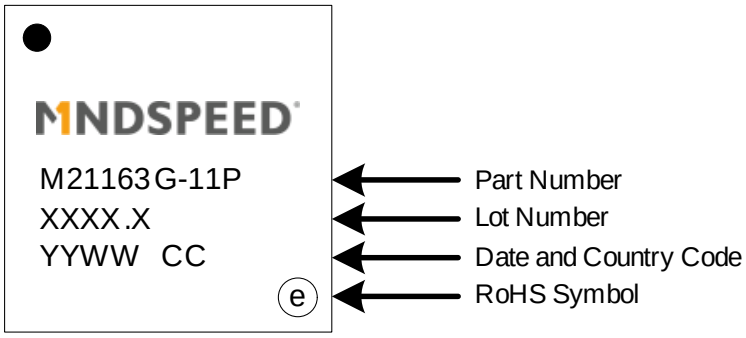
Ordering Information

Part Number	Package	Operating Temperature
M21163G-11P	17 mm x 17 mm, 252-pin, BGA package	-40 °C to 85 °C
* The letter “G” designator after the part number indicates that the device is RoHS compliant. Refer to www.mindspeed.com for additional information.		

Revision History

Revision	Level	Date	Description
B	Advance	September 2011	Updated Chipcode register E1h.
A	Advance	August 2011	Initial release.

M21163 Marking Diagram



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1.0 Electrical Characteristics

Unless noted otherwise, specifications in this chapter apply to the recommended operation conditions outlined in Table 1-2, PRBS 2^{10} – 1 test pattern at 3.2 Gbps, R_{LOAD} = 50 Ω.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Note	Minimum	Maximum	Unit
AV_{DDCORE}	Analog Core Supply Voltage	1, 2	-0.5	1.5	V
AV_{DDIO}	Analog Input/Output Supply Voltage (reconfigurable)	1, 2	-0.5	3.6	V
AV_{DDO}	Analog Output Supply Voltage (dedicated outputs)	1, 2	-0.5	3.6	V
DV_{DDIO}	Digital Input/Output Supply Voltage	1, 2	-0.5	3.6	V
$V_{IN,PCML}$	DC Input Voltage (PCML)	1, 2	V_{SS} - 0.5	AV_{DDIO} + 0.5	V
$V_{IN,CMOS}$	DC Input Voltage (CMOS)	1, 2	V_{SS} - 0.5	DV_{DDIO} + 0.5	V
T_{STORE}	Storage temperature	1, 2	-65	150	°C
T_{JUNC}	Junction temperature	1, 2		125	°C
$V_{ESD,HBM}$	Electrostatic discharge, Human Body Model (HBM)	1, 2	TBD	TBD	V
$V_{ESD,CDM}$	Electrostatic discharge, Charged Device Model (CDM)	1, 2	TBD	TBD	V

NOTES:

1. Exposure of the device beyond the minimum/maximum limits may cause permanent damage.
2. Limits listed in the above table are stress limits only and do not imply functional operation within these limits.

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
AV_{DDCORE}	Analog Core Supply Voltage	—	1.14	1.2	1.26	V
AV_{DDIO}	Analog Input/Output Supply Voltage	—	1.14	1.2,1.8,2.5,3.3	3.47	V
AV_{DDO}	Analog Output Supply Voltage	—	1.14	1.2,1.8,2.5,3.3	3.47	V
DV_{DDIO}	Digital Input/Output Supply Voltage	—	1.14	1.2,1.8,2.5,3.3	3.47	V
T_{CASE}	Case Temperature	1, 3	-40	—	+85	°C
θ_{JC}	Junction to Case Thermal Resistance	2, 3	—	6.0	—	°C/W

NOTES:

1. Lower limit is ambient temperature and upper limit is case temperature.
2. Without heat sink and without airflow. Junction temperature must not exceed 110 °C.
3. T_{JUNC} is not equal to T_{CASE} + (θ_{JC} * Power Consumption). The actual thermal resistance depends on the amount of heat flowing directly on the case versus the amount of heat flowing through the exposed ground pad on the board. The heat flow is affected by the board design, air flow and heat sink.

Table 1-3. Power Consumption Specifications

Symbol	Parameter			Typical	Maximum	Unit
DI_{DDIO}	DV_{DDIO} Current Consumption, Average current using the SPI interface in Read mode at maximum speed		DV_{DDIO} = 1.2 V	1	TBD	mA
			DV_{DDIO} = 1.8 V	1.2	TBD	mA
			DV_{DDIO} = 2.5 V	1.6	TBD	mA
			DV_{DDIO} = 3.3 V	2.1	TBD	mA
AI_{DDI}	AV_{DDIO} Current Consumption per AV_{DDIO} used as an Input	AC coupled	AV_{DDIO} = 1.2 V	0.5	TBD	mA
			AV_{DDIO} = 1.8 V	1.5	TBD	mA
			AV_{DDIO} = 2.5 V	3	TBD	mA
			AV_{DDIO} = 3.3 V	4	TBD	mA
AI_{DDO}	AV_{DDIO} Current Consumption per AV_{DDO}/ AV_{DDIO} used as an Output	Minimum swing AC coupled	AV_{DDIO} = 1.2 V	15	TBD	mA
			AV_{DDIO} = 1.8 V	15	TBD	mA
			AV_{DDIO} = 2.5 V	16	TBD	mA
			AV_{DDIO} = 3.3 V	17	TBD	mA
		Intermediate swing AC coupled	AV_{DDIO} = 1.2 V	18	TBD	mA
			AV_{DDIO} = 1.8 V	19	TBD	mA
			AV_{DDIO} = 2.5 V	20	TBD	mA
			AV_{DDIO} = 3.3 V	21	TBD	mA
		Maximum swing AC coupled	AV_{DDIO} = 1.2 V	26	TBD	mA
			AV_{DDIO} = 1.8 V	28	TBD	mA
			AV_{DDIO} = 2.5 V	28	TBD	mA
			AV_{DDIO} = 3.3 V	29	TBD	mA
AI_{DDCORE}	AV_{DDCORE} Current Consumption		AV_{DDCORE} = 1.2 V	20x (Active Inputs) + 18.2x (Active Outputs) + 25	24x (Active Inputs) + 25.7x (Active Outputs) + 30	mA
P_{TOTAL}	Total Power Consumption		$P_{Total}(mW) = \sum_{n}^{TotalInputs}(AV_{DDIO\,n} \times AI_{DDI\,n}) + \sum_{m}^{TotalOutputs}(AV_{DDO\,m} \times AI_{DDO\,m}) + AV_{DDCORE} \times AI_{DDCORE} + DV_{DDIO} \times DI_{DDIO}$			mW

NOTES:

1. The total power consumption for the M21163 depends on the number of inputs and outputs the designer has selected.
2. It is not recommended to have more than 24 ports setup as outputs with maximum output swing when AV_{DDIO} = 3.3 V due to high power consumption.

Table 1-4. PCML Input/Output Electrical Characteristics

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
DR	NRZ input data rate	—	143	—	3200	Mbps
DR	NRZ input data rate	9	0.01	—	143	Mbps
V_{IN}	Differential input swing	1, 12	300	800	2000	mV_{PPD}
V_{ICM}	Input common mode voltage	1	AV_{DDIO} - 0.5	—	AV_{DDIO} + 0.1	V
IE	Input Equalization	—	—	0 dB to 6 dB, 8 steps	—	dB
R_{IN}	Input Single Ended Termination Resistance	2	45	50	55	Ω
V_{OUT}	Differential Output - low	4	TBD	600	TBD	mV_{PPD}
	Differential Output - medium	4, 5	TBD	800	TBD	mV_{PPD}
	Differential Output - high	4, 10	TBD	TBD	TBD	mV_{PPD}
	Differential Output - high	4, 11	TBD	1200	TBD	mV_{PPD}
R_{OUT}	Output Single Ended termination resistance	3	45	50	55	Ω
t_R/t_F	Output Rise/Fall Time (20%-80%)	6	—	120	—	ps
DE	Output de-emphasis settings	4, 6	—	0, 2, 4, 6	—	dB
t_{DCV}	Output Duty Cycle Variation from ideal	4, 8, 12	—	—	20	ps
t_{JIT}	Total jitter added (t_{RJ} and t_{DJ})	4, 5, 7	—	—	300	mUI

NOTES:

1. Value specified at the device pins.
2. Internal termination to AV_{DDIO}.
3. Internal termination to AV_{DDIO} or AV_{DDO}.
4. Measured into 50 Ω load, 100 Ω differential.
5. Default output swing level.
6. Measured with 16 ones and 16 zeros pattern.
7. Launch across backplane or JBERT trace. Measured to BER 1E-12 using PRBS10 test pattern at 3.2 Gbps and 32 inches of JBERT trace from Agilent JBERT or equivalent.
8. Value as reported by Agilent DCAJ or equivalent; test system jitter not included.
9. DC offset correction loops and LOS disabled.
10. AV_{DDIO}/AV_{DDIO} = 1.2 V.
11. $AV_{DDIO}/AV_{DDIO} \geq$ 1.8 V.
12. Measured to BER 1E-12 using PRBS10 test pattern at 3.2 Gbps.

Table 1-5. Control/Interface Logic Input/Output Characteristics

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
V_{OH}	High level output voltage	1	0.8 x DV_{DDO}	DV_{DDO}	—	V
V_{OL}	Low level output voltage	2	—	0	0.2 x DV_{DDO}	V
V_{IH}	High level input voltage	1	0.75 x DV_{DDO}	—	DV_{DDO}	V
V_{IL}	Low level input voltage	1	0	—	0.25 x DV_{DDO}	V

NOTES:

1. I_{OH} = -2 mA for DV_{DDO} = 1.2V. - 3 mA for $DV_{DDO} \geq$ 1.8V.
2. I_{OL} = 2 mA for DV_{DDO} = 1.2V. 3 mA for $DV_{DDO} \geq$ 1.8V.

2.0 Typical Performance Characteristics

Figure 2-1. M21163 Total Typical Power Consumption (mW) vs. Crosspoint Configuration

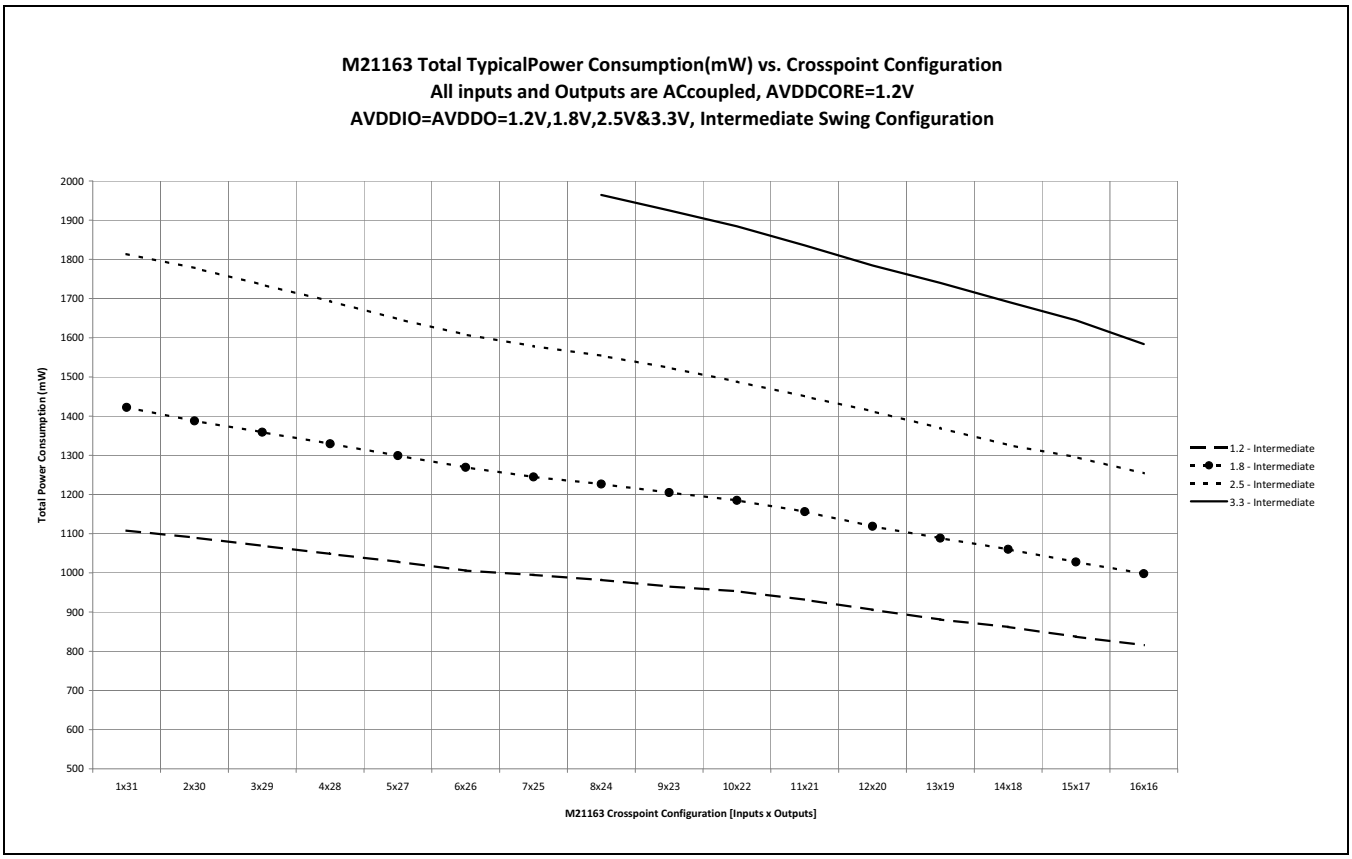


Figure 2-2. M21163 Total Jitter (mUI) vs. Trace Length vs. Equalization Level with 800 mV_{PPD} Input Swing at Launch

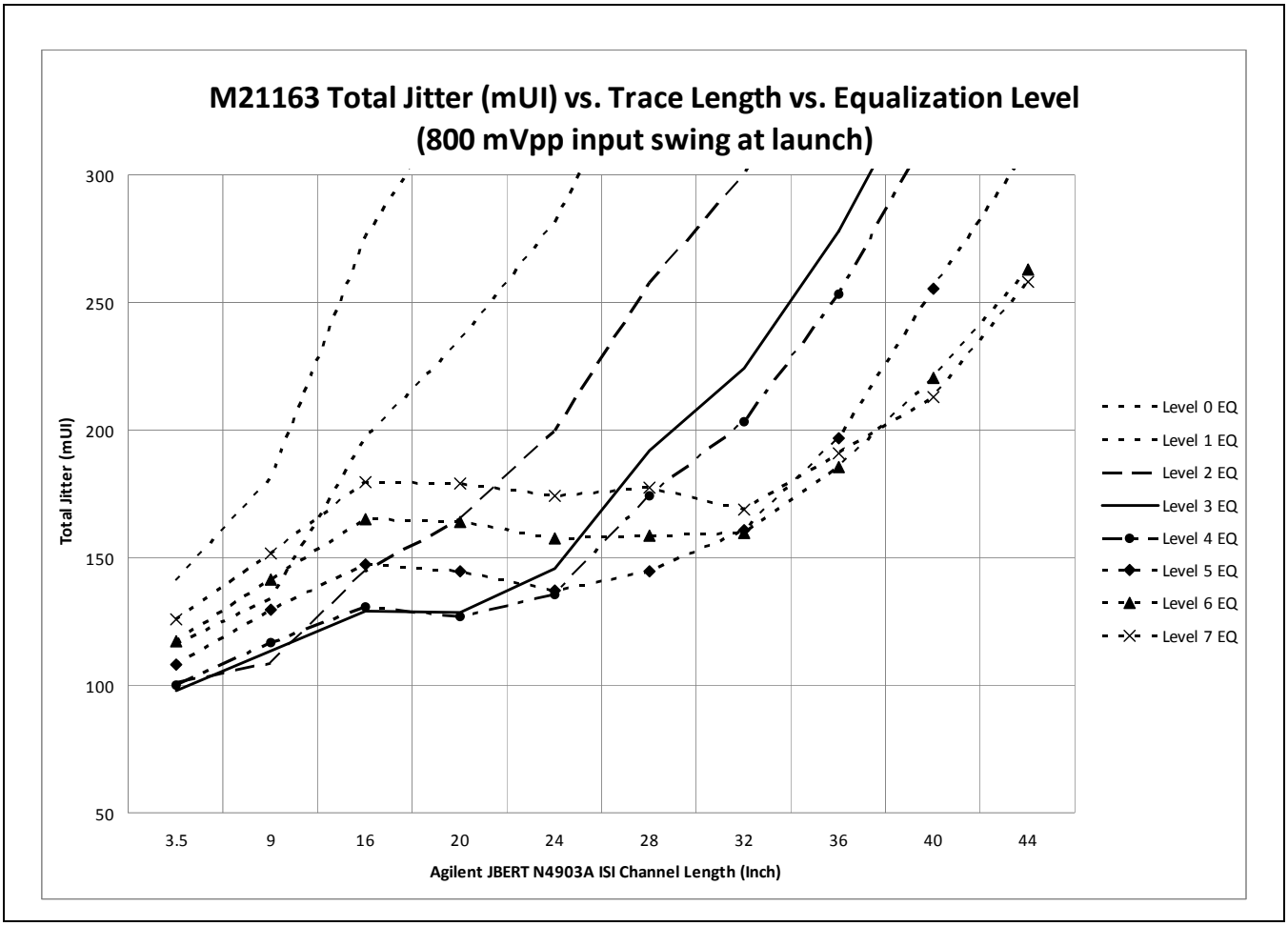
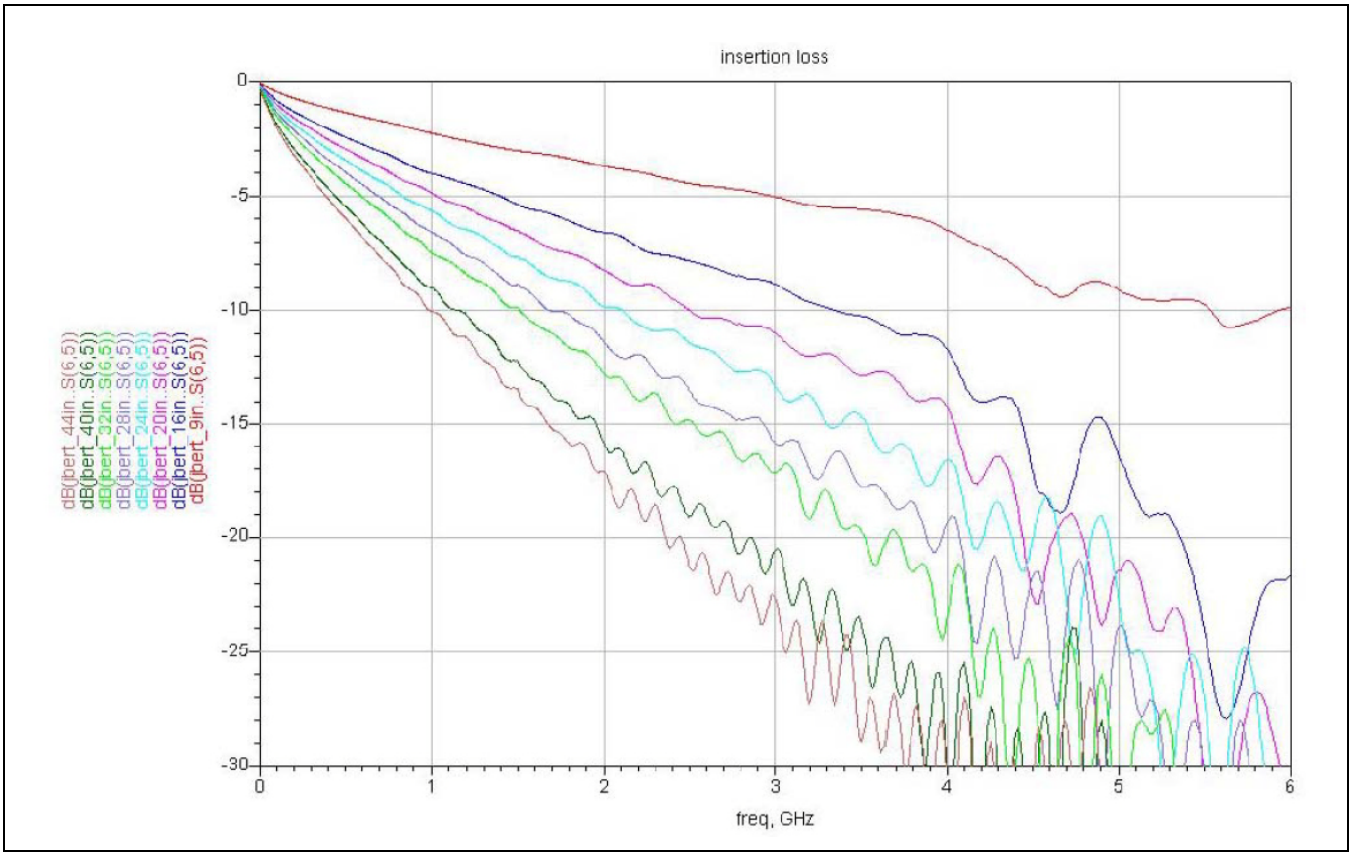


Figure 2-3. Agilent BERT N4903A FR4 Backplane Insertion Loss. These Backplane Traces were Used to Measure Input EQ on Figure 2-2



3.0 Pinout Diagram, Pin Descriptions, and Package Outline Drawing

The M21163 is offered in a green and RoHS compliant 17 mm x 17 mm, 252-pin, thermally enhanced BGA package. The pinout for the M21163 is shown in Figure 3-1.

Figure 3-1. M21163 Pinout Diagram (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A		DIO6N	DIO6P	VSS	DIO5N	DIO5P	VSS	DIO4N	DIO4P	VSS	DIO2N	DIO2P	VSS	DIO1N	DIO1P		A
B	DIO9P	VSS	AVDDIO6	AVDDIO7	VSS	VSS	AVDDIO5	AVDDIO4	AVDDIO3	AVDDIO2	VSS	VSS	AVDDIO0	AVDDIO1	VSS	DOUT30P	B
C	DIO9N	AVDDIO9	VSS	VSS	DIO7N	DIO7P	VSS	DIO3N	DIO3P	VSS	DIO0N	DIO0P	VSS	MF3	AVDDO30_31	DOUT30N	C
D	VSS	AVDDIO8	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	MF4	VSS	VSS	VSS	D
E	DIO10P	VSS	DIO8P	VSS	VSS	AVDDCORE	AVDDCORE	AVDDCORE	AVDDCORE	AVDDCORE	AVDDCORE	MF5	MF1	DOUT31P	AVDDO30_31	DOUT29P	E
F	DIO10N	VSS	DIO8N	VSS	AVDDCORE	VSS	VSS	VSS	VSS	VSS	VSS	AVDDCORE	VSS	DOUT31N	VSS	DOUT29N	F
G	VSS	AVDDIO10	VSS	VSS	AVDDCORE	VSS	VSS	VSS	VSS	VSS	VSS	AVDDCORE	VSS	VSS	AVDDO28_29	AVDDO28_29	G
H	DIO12P	AVDDIO11	DIO11P	VSS	AVDDCORE	VSS	VSS	VSS	VSS	VSS	VSS	DVDDIO	VSS	DOUT27P	VSS	DOUT28P	H
J	DIO12N	AVDDIO12	DIO11N	VSS	AVDDCORE	VSS	VSS	VSS	VSS	VSS	VSS	DVDDIO	VSS	DOUT27N	VSS	DOUT28N	J
K	VSS	AVDDIO13	VSS	VSS	AVDDCORE	VSS	VSS	VSS	VSS	VSS	VSS	AVDDCORE	VSS	VSS	AVDDO26_27	AVDDO26_27	K
L	DIO13P	VSS	DIO15P	VSS	AVDDCORE	VSS	VSS	VSS	VSS	VSS	VSS	AVDDCORE	VSS	DOUT24P	VSS	DOUT26P	L
M	DIO13N	VSS	DIO15N	VSS	VSS	AVDDCORE	AVDDCORE	AVDDCORE	AVDDCORE	AVDDCORE	AVDDCORE	MF2	MF0	DOUT24N	AVDDO24_25	DOUT26N	M
N	VSS	AVDDIO15	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	MF6	VSS	VSS	VSS	N
P	DIO14P	AVDDIO14	VSS	VSS	DIO16N	DIO16P	VSS	DIO19N	DIO19P	VSS	DIO23N	DIO23P	VSS	MF7	AVDDO24_25	DOUT25P	P
R	DIO14N	VSS	AVDDIO17	AVDDIO16	VSS	VSS	AVDDIO18	AVDDIO19	AVDDIO20	AVDDIO21	VSS	VSS	AVDDIO23	AVDDIO22	VSS	DOUT25N	R
T		DIO17N	DIO17P	VSS	DIO18N	DIO18P	VSS	DIO20N	DIO20P	VSS	DIO21N	DIO21P	VSS	DIO22N	DIO22P		T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Table 3-1. M21163 Pin Descriptions

Pin Name	Pin Number(s)	Type	Description
DV_{DDIO}	H12, J12	Power	Digital Positive Supply
AV_{DDCORE}	E6, E7, E8, E9, E10, E11, F5, F12, G5, G12, H5, J5, K5, K12, L5, L12, M6, M7, M8, M9, M10, M11	Power	Analog Positive Supply
$AV_{DDIO}0$	B13	Power	Analog Positive Supply
$AV_{DDIO}1$	B14	Power	Analog Positive Supply
$AV_{DDIO}2$	B10	Power	Analog Positive Supply
$AV_{DDIO}3$	B9	Power	Analog Positive Supply
$AV_{DDIO}4$	B8	Power	Analog Positive Supply
$AV_{DDIO}5$	B7	Power	Analog Positive Supply
$AV_{DDIO}6$	B3	Power	Analog Positive Supply
$AV_{DDIO}7$	B4	Power	Analog Positive Supply
$AV_{DDIO}8$	D2	Power	Analog Positive Supply
$AV_{DDIO}9$	C2	Power	Analog Positive Supply
$AV_{DDIO}10$	G2	Power	Analog Positive Supply
$AV_{DDIO}11$	H2	Power	Analog Positive Supply
$AV_{DDIO}12$	J2	Power	Analog Positive Supply
$AV_{DDIO}13$	K2	Power	Analog Positive Supply
$AV_{DDIO}14$	P2	Power	Analog Positive Supply
$AV_{DDIO}15$	N2	Power	Analog Positive Supply
$AV_{DDIO}16$	R4	Power	Analog Positive Supply
$AV_{DDIO}17$	R3	Power	Analog Positive Supply
$AV_{DDIO}18$	R7	Power	Analog Positive Supply
$AV_{DDIO}19$	R8	Power	Analog Positive Supply
$AV_{DDIO}20$	R9	Power	Analog Positive Supply
$AV_{DDIO}21$	R10	Power	Analog Positive Supply
$AV_{DDIO}22$	R14	Power	Analog Positive Supply
$AV_{DDIO}23$	R13	Power	Analog Positive Supply
$AV_{DDO}24\_25$	M15, P15	Power	Analog Positive Supply
$AV_{DDO}26\_27$	K15, K16	Power	Analog Positive Supply
$AV_{DDO}28\_29$	G15, G16	Power	Analog Positive Supply
$AV_{DDO}30\_31$	C15, E15	Power	Analog Positive Supply

Table 3-1. M21163 Pin Descriptions

Pin Name	Pin Number(s)	Type	Description
V_{SS}	A4, A7, A10, A13, B2, B5, B6, B11, B12, B15, C3, C4, C7, C10, C13, D1, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D14, D15, D16, E2, E4, E5, F2, F4, F6, F7, F8, F9, F10, F11, F13, F15, G1, G3, G4, G6, G7, G8, G9, G10, G11, G13, G14, H4, H6, H7, H8, H9, H10, H11, H13, H15, J4, J6, J7, J8, J9, J10, J11, J13, J15, K1, K3, K4, K6, K7, K8, K9, K10, K11, K13, K14, L2, L4, L6, L7, L8, L9, L10, L11, L13, L15, M2, M4, M5, N1, N3, N4, N5, N6, N7, N8, N9, N10, N11, N12, N14, N15, N16, P3, P4, P7, P10, P13, R2, R5, R6, R11, R12, R15, T4, T7, T10, T13	Power	Ground
DIO0P,DIO0N	C12, C11	PCML input/output	Data Input/Output Lane0; true/ complement
DIO1P,DIO1N	A15, A14	PCML input/output	Data Input/Output Lane1; true/ complement
DIO2P,DIO2N	A12, A11	PCML input/output	Data Input/Output Lane2; true/ complement
DIO3P,DIO3N	C9, C8	PCML input/output	Data Input/Output Lane3; true/ complement
DIO4P,DIO4N	A9, A8	PCML input/output	Data Input/Output Lane4; true/ complement
DIO5P,DIO5N	A6, A5	PCML input/output	Data Input/Output Lane5; true/ complement
DIO6P,DIO6N	A3, A2	PCML input/output	Data Input/Output Lane6; true/ complement
DIO7P,DIO7N	C6, C5	PCML input/output	Data Input/Output Lane7; true/ complement
DIO8P,DIO8N	E3, F3	PCML input/output	Data Input/Output Lane8; true/ complement
DIO9P,DIO9N	B1, C1	PCML input/output	Data Input/Output Lane9; true/ complement
DIO10P,DIO10N	E1, F1	PCML input/output	Data Input/Output Lane10; true/ complement
DIO11P,DIO11N	H3, J3	PCML input/output	Data Input/Output Lane11; true/ complement
DIO12P,DIO12N	H1, J1	PCML input/output	Data Input/Output Lane12; true/ complement
DIO13P,DIO13N	L1, M1	PCML input/output	Data Input/Output Lane13; true/ complement
DIO14P,DIO14N	P1, R1	PCML input/output	Data Input/Output Lane14; true/ complement

Table 3-1. M21163 Pin Descriptions

Pin Name	Pin Number(s)	Type	Description
DIO15P,DIO15N	L3, M3	PCML input/output	Data Input/Output Lane15; true/ complement
DIO16P,DIO16N	P6, P5	PCML input/output	Data Input/Output Lane16; true/ complement
DIO17P,DIO17N	T3, T2	PCML input/output	Data Input/Output Lane17; true/ complement
DIO18P,DIO18N	T6, T5	PCML input/output	Data Input/Output Lane18; true/ complement
DIO19P,DIO19N	P9, P8	PCML input/output	Data Input/Output Lane19; true/ complement
DIO20P,DIO20N	T9, T8	PCML input/output	Data Input/Output Lane20; true/ complement
DIO21P,DIO21N	T12, T11	PCML input/output	Data Input/Output Lane21; true/ complement
DIO22P,DIO22N	T15, T14	PCML input/output	Data Input/Output Lane22; true/ complement
DIO23P,DIO23N	P12, P11	PCML input/output	Data Input/Output Lane23; true/ complement
DOUT24P,DOUT24N	L14, M14	PCML output	Data Output Lane24; true/ complement
DOUT25P,DOUT25N	P16, R16	PCML output	Data Output Lane25; true/ complement
DOUT26P,DOUT26N	L16, M16	PCML output	Data Output Lane26; true/ complement
DOUT27P,DOUT27N	H14, J14	PCML output	Data Output Lane27; true/ complement
DOUT28P,DOUT28N	H16, J16	PCML output	Data Output Lane28; true/ complement
DOUT29P,DOUT29N	E16, F16	PCML output	Data Output Lane29; true/ complement
DOUT30P,DOUT30N	B16, C16	PCML output	Data Output Lane30; true/ complement
DOUT31P,DOUT31N	E14, F14	PCML output	Data Output Lane31; true/ complement
MF1,MF0	E13, M13	CMOS Control Input	LL = 4-wire digital interface selected LH = JTAG digital interface selected HL = 2-wire digital interface selected HH = Not used Note: Any changes on MF[1:0] will perform a reset.
MF2	M12	CMOS Control Input	2-wire: Device Address 0 4-wire: xCS JTAG: TDI

Table 3-1. M21163 Pin Descriptions

Pin Name	Pin Number(s)	Type	Description
MF3	C14	CMOS Control Input	2-wire: Device Address 1 4-wire: SI
MF4	D13	CMOS Control Input/Output	2-wire: SDA 4-wire: SO JTAG: TMS
MF5	E12	CMOS Control Input	2-wire: SCL 4-wire: SCLK JTAG: TCLK
MF6	N13	CMOS Control Input/Output	2-wire: xSET 4-wire: xSET JTAG: TDO
MF7	P14	CMOS Control Output	xAlarm

Figure 3-2. PCML Input

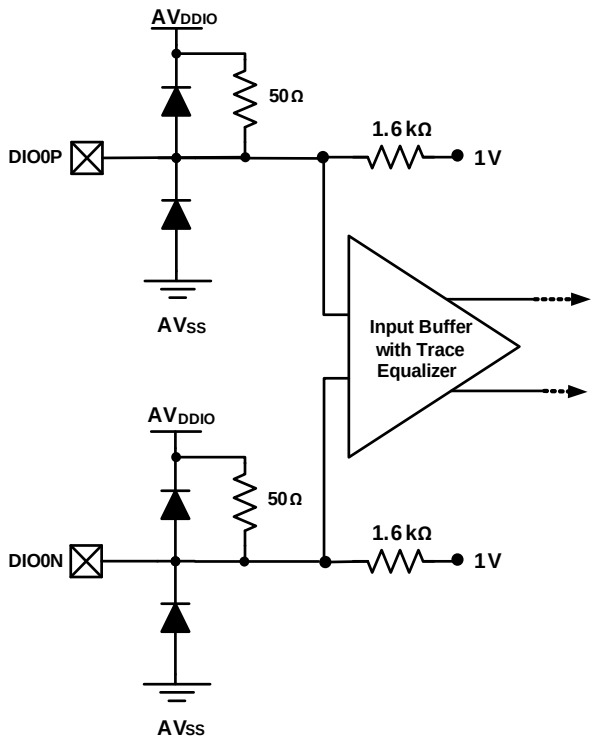


Figure 3-3. PCML Output

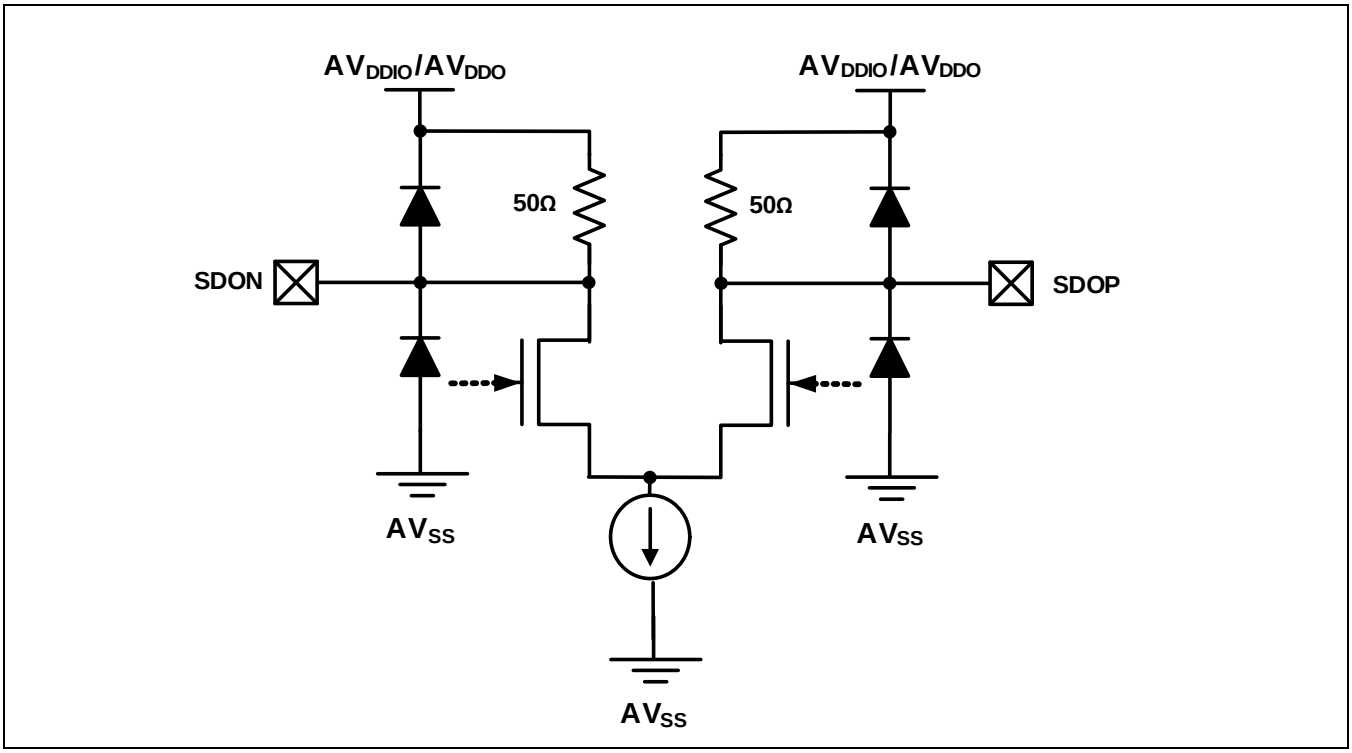


Figure 3-4. I-Digital with No Pull-up or Pull-down

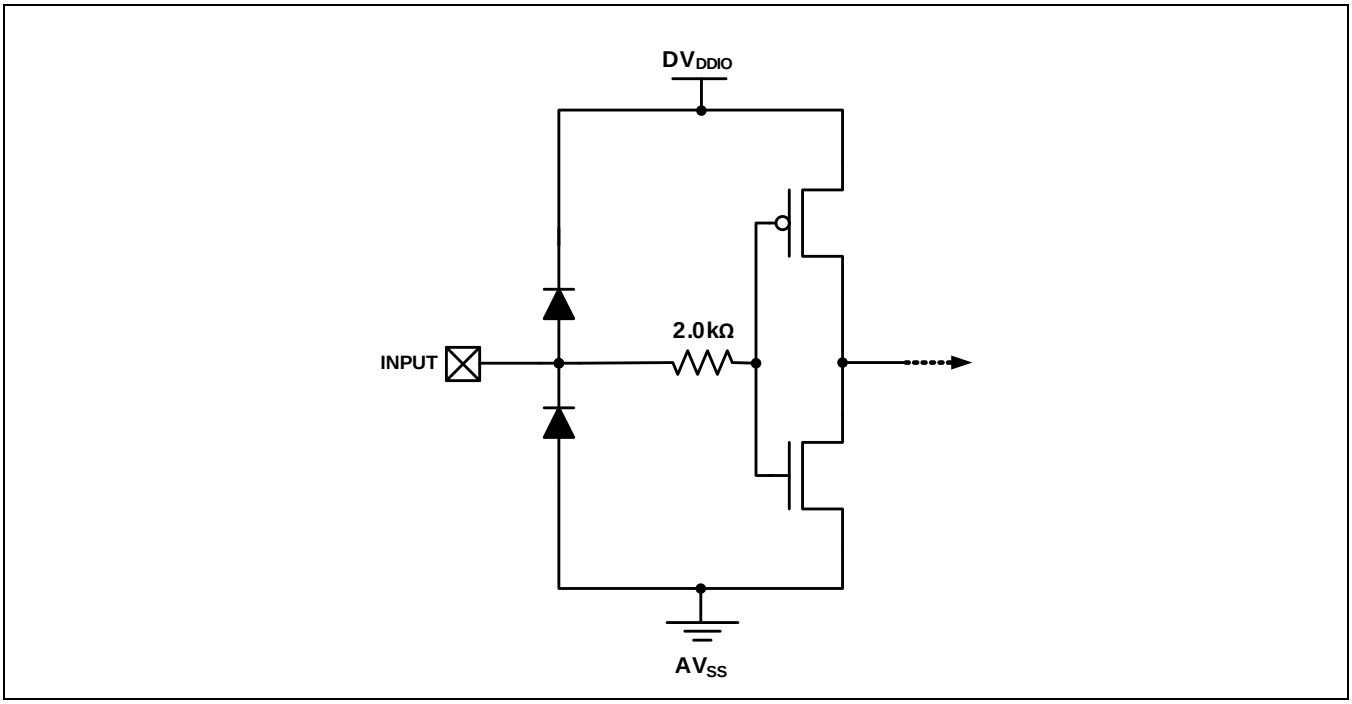


Figure 3-5. I-Digital With Pull-up

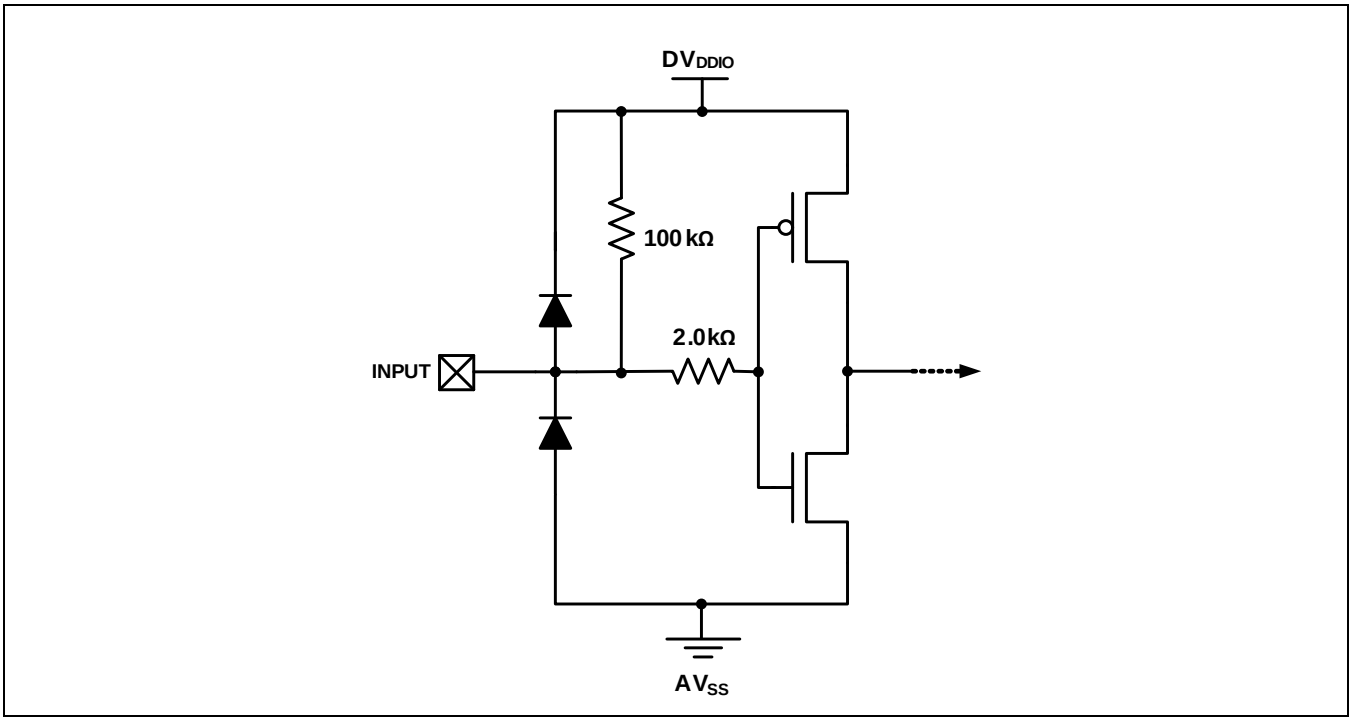


Figure 3-6. I-Digital With Pull-down

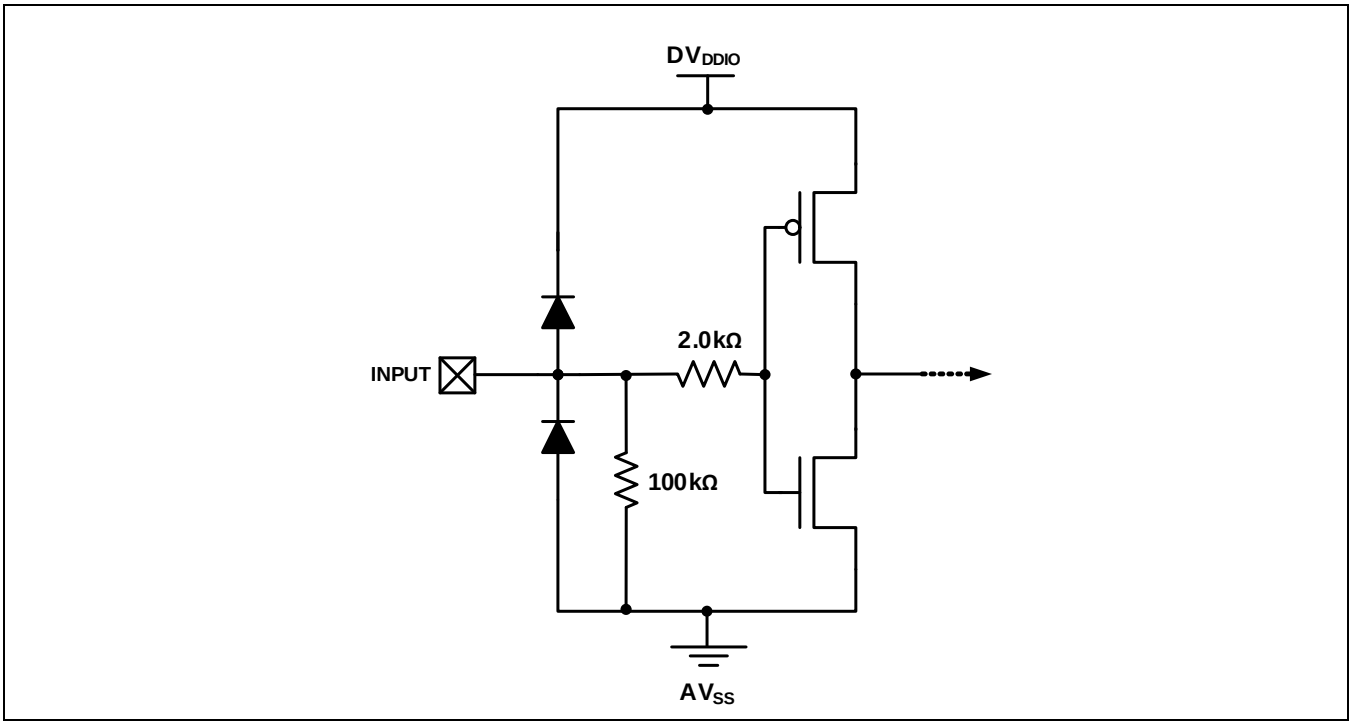


Figure 3-7. 3-State/I-Digital

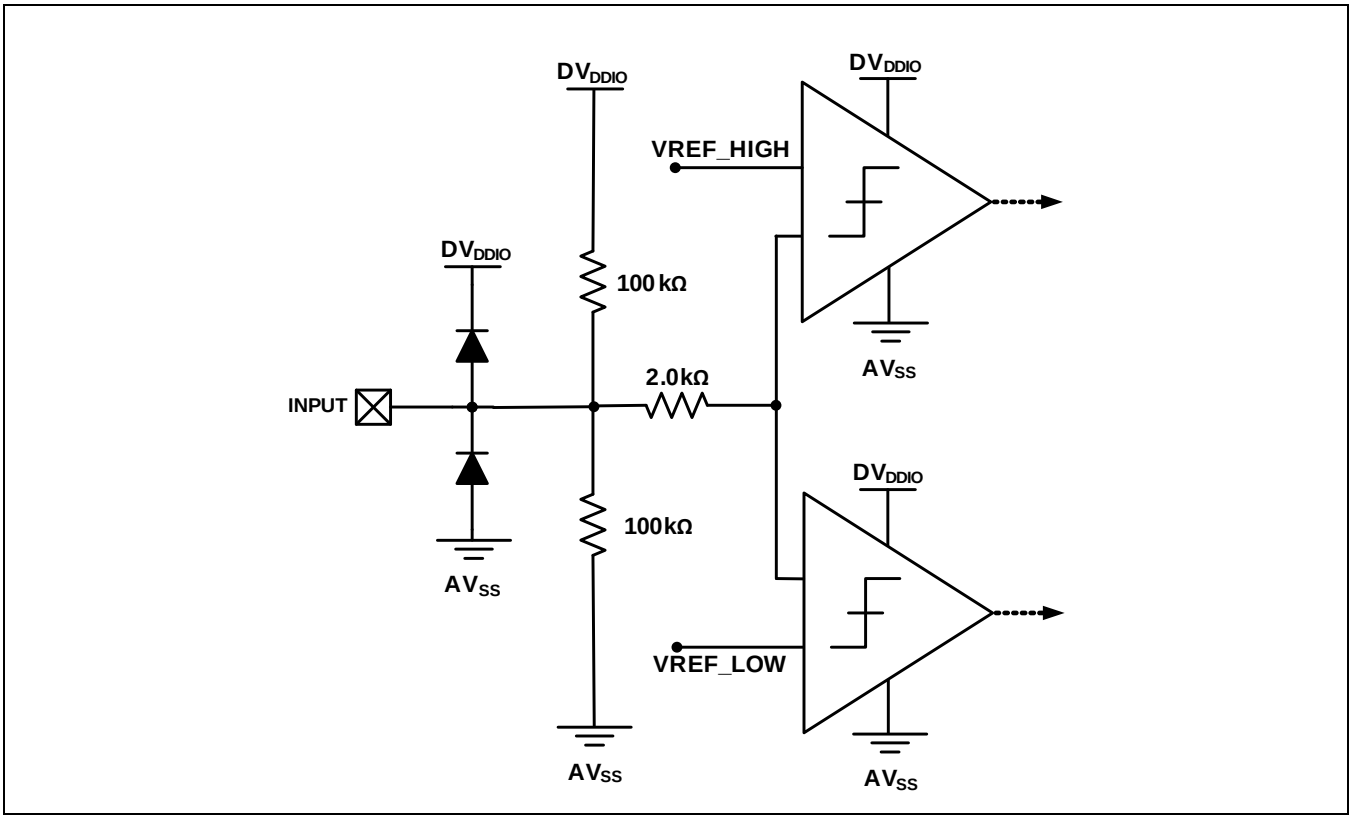


Figure 3-8. O-Digital

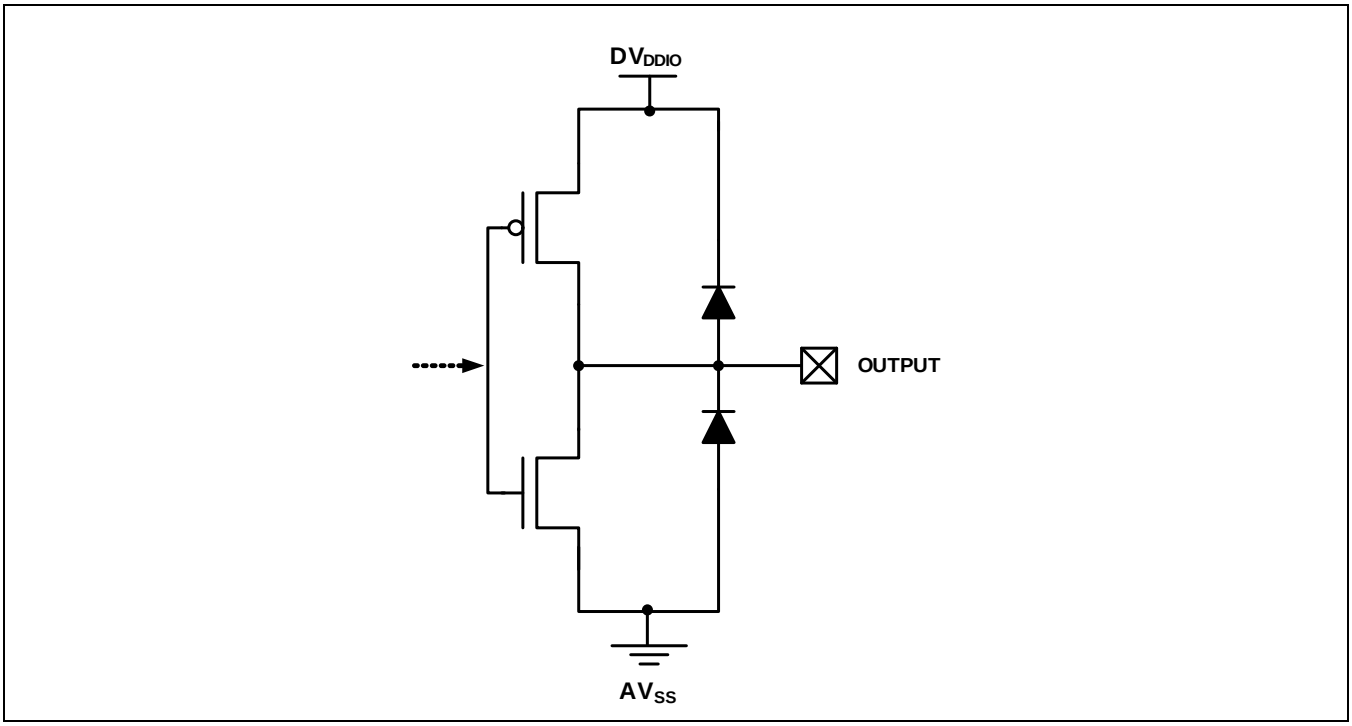


Figure 3-9. O-Open Drain

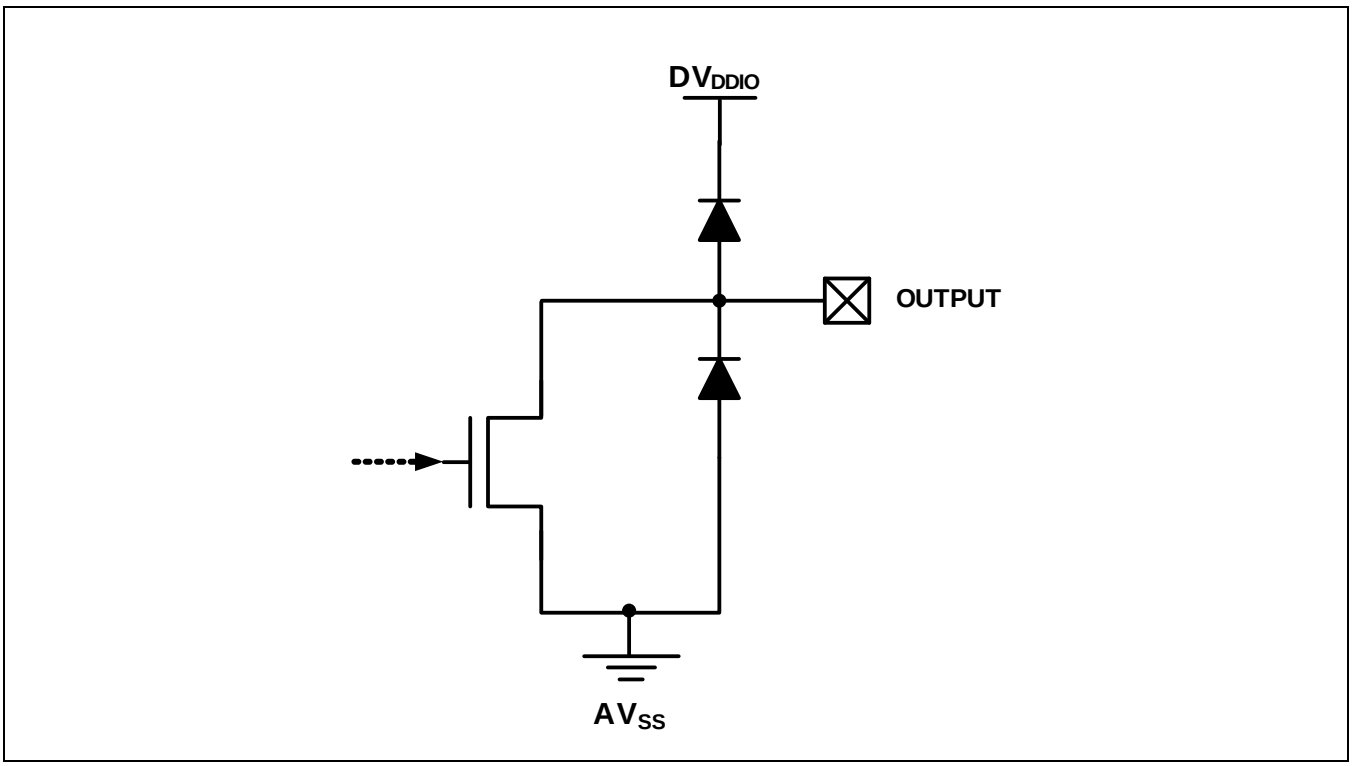
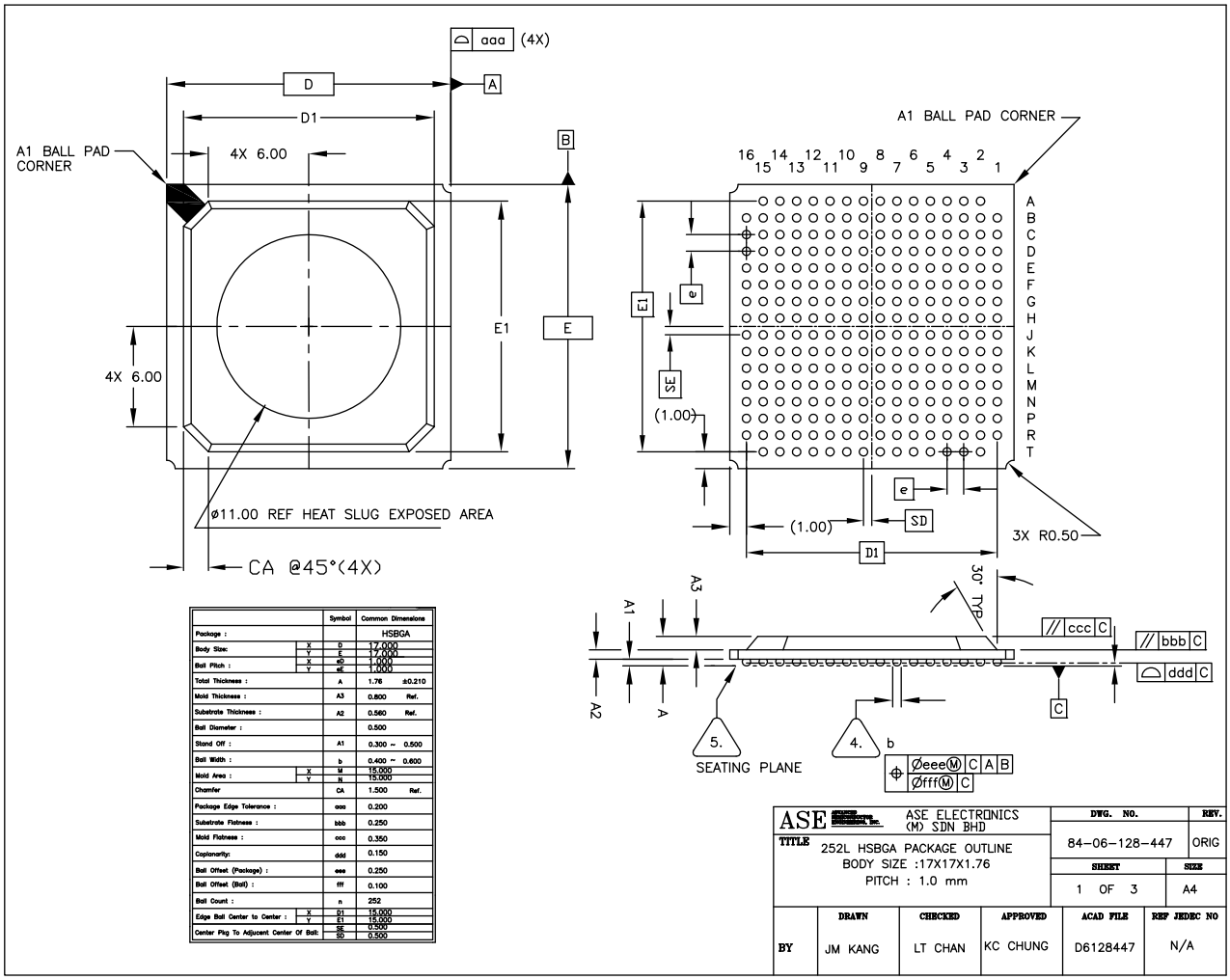


Figure 3-10. M21163 Package Outline Drawing



		Symbol	Common Dimensions
Package :			HSBGA
Body Size:	X	D	17.000
	Y	E	17.000
Ball Pitch :	X	eD	1.000
	Y	eE	1.000
Total Thickness :		A	1.76 ±0.210
Mold Thickness :		A3	0.800 Ref.
Substrate Thickness :		A2	0.560 Ref.
Ball Diameter :			0.500
Stand Off :		A1	0.300 ~ 0.500
Ball Width :		b	0.400 ~ 0.600
Mold Area :	X	M	15.000
	Y	N	15.000
Chamfer		CA	1.500 Ref.
Package Edge Tolerance :		aaa	0.200
Substrate Flatness :		bbb	0.250
Mold Flatness :		ccc	0.350
Coplanarity:		ddd	0.150
Ball Offset (Package) :		eee	0.250
Ball Offset (Ball) :		fff	0.100
Ball Count :		n	252
Edge Ball Center to Center :	X	D1	15.000
	Y	E1	15.000
Center Pkg To Adjucent Center Of Ball:		SE	0.500
		SD	0.500

ASE — ASE ELECTRONICS (M) SDN BHD				DWG. NO.	REV.
TITLE: 252L HSBGA PACKAGE OUTLINE BODY SIZE :17X17X1.76 PITCH : 1.0 mm				84-06-128-447	ORIG
				SHEET: 1 OF 3	SIZE: A4
BY	DRAWN	CHECKED	APPROVED	ACAD FILE	REF JEDEC NO
	JM KANG	LT CHAN	KC CHUNG	D6128447	N/A

NOTES :

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. SOLDER BALL POSITION DESIGNATION PER JESD 95–1, SPP–010.
3. THIS DIMENSION INCLUDES STAND–OFF HEIGHT, PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES, E.G., EXTERNAL HEATSINK OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AN ATTACHED FEATURE.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

4.0 Functional Description

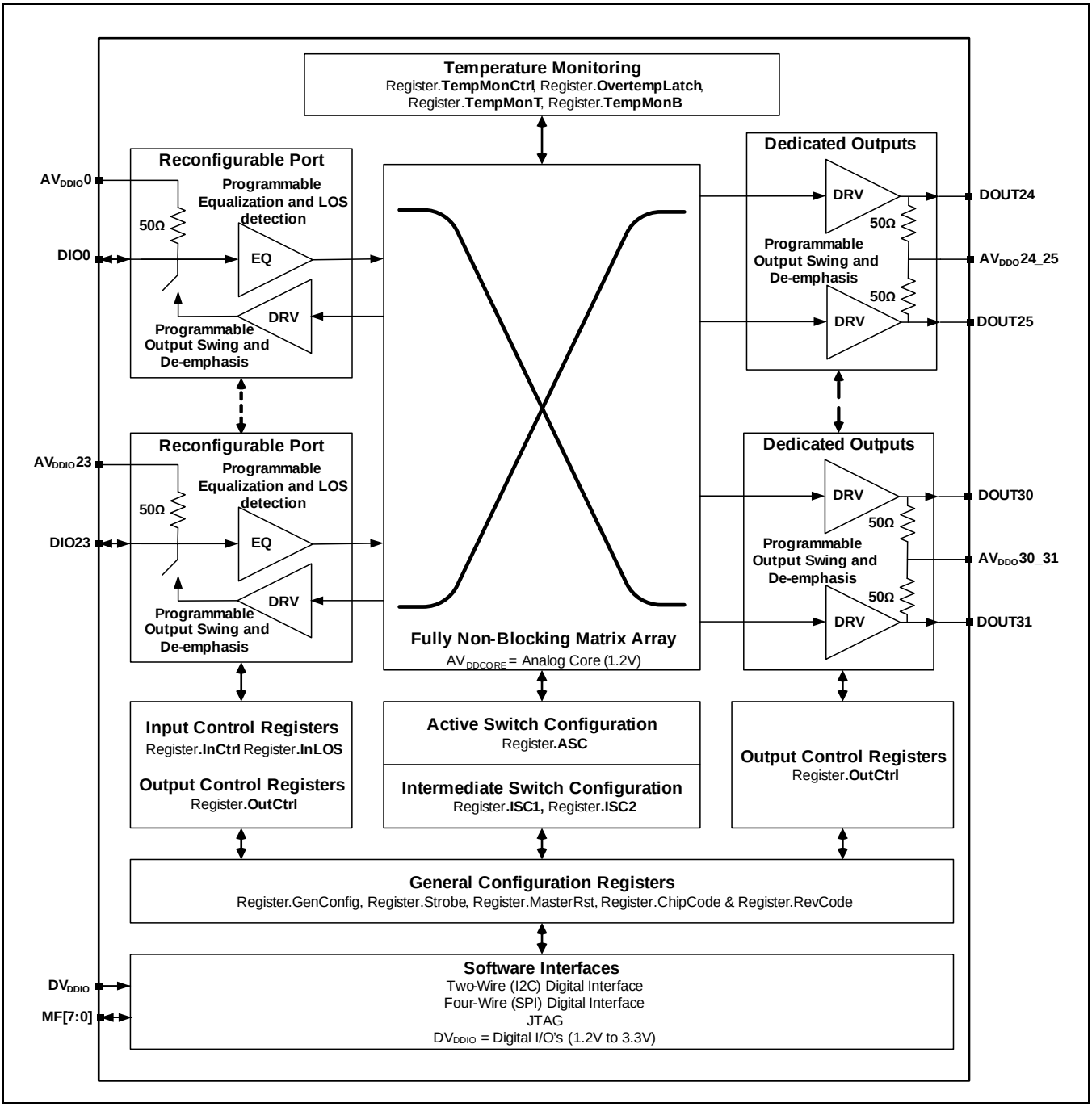
The M21163 is a 32 port reconfigurable non-blocking asynchronous crosspoint switch capable of robust operation at data rates up to 3.2 Gbps. In order to allow for synchronous switching, the crosspoint core can be configured by two pre-programmed switch states, or intermediate switch configurations, ISC. Changing the switch state may be triggered using the hardware pin xSETs or registers bits. Alternatively, the switch may be configured in direct access mode, in which all states take effect immediately after programming.

Advanced programmable signal conditioning in the form of input equalization and output de-emphasis are provided to improve performance in large, high data rate systems. The M21163 also includes a Loss of Signal (LOS) detector on each input lane that can used to squelch the output preventing unwanted chatter.

The M21163 is designed to be compatible with multiple protocol standards such as Serial Digital Interface (SDI) video, InfiniBand, Fibre Channel, XAUI GbE, parallel 10GbE and SONET. The various options of the device and the switch state can be configured with registers accessed through a 2-wire (I^2C compatible) or a 4-wire SPI interface.

The following figure depicts the functional block diagram of the M21163. The various functions and blocks are described in detail in the subsequent sections.

Figure 4-1. M21163 Functional Block Diagram



4.1 Power Up

4.1.1 Power on Reset

The M21163 initiates a power-on reset upon application of supply power at pin.AV_{DDCORE}. A software reset can also be invoked by writing the value AAh to register.**MasterRst** (address.E0h). Alternatively, the device may be reset through hardware by changing the logic state of pin.**MF**[1:0]. All resets are functionally equivalent. After a reset event, all registers are set to their default state as described in Section 5.0.

By default, the device is configured after power up, hardware, software power down, or software reset as defined below:

- All input buffers are powered down. The differential input to the buffers are terminated to 50 Ω resistors to AV_{DDIO}.
- All dedicated and non-dedicated output buffers are powered down. The dedicated differential outputs are pulled to AV_{DDO} via 50 Ω resistors.
- Crosspoint core is not configured; i.e. no input is mapped to no output. A valid configuration needs to be set by programming register.**ASC** after power up.

4.1.2 Power up Sequence

The M21163 has four different power supplies: AV_{DDIO} (per configurable IO), AV_{DDO}, AV_{DDCORE}, and DV_{DDIO}.

It is recommended to power up DV_{DDIO} are set as AV_{DDCORE} whenever possible; this is easily accomplished if AV_{DDCORE} = DV_{DDIO} = 1.2 V. For DV_{DDIO} voltages greater than 1.2 V, two different power supplies are needed and it may be difficult to power up DV_{DDIO} and AV_{DDCORE} at the same time. In this case it is recommended to have DV_{DDIO} supplied before or with AV_{DDCORE}, to avoid control register corruption. If DV_{DDIO} is supplied after AV_{DDCORE}, a hardware or software reset is needed to make sure all the registers hold their default value. This reset is needed due to the Power-on Reset (POR) being triggered by AV_{DDCORE}, so if AV_{DDCORE} is supplied before DV_{DDIO}, the digital engine does not receive the reset.

There is no power sequence needed for AV_{DDIO} or AV_{DDO}, they can be supplied shortly after or before AV_{DDCORE} or DV_{DDIO}.

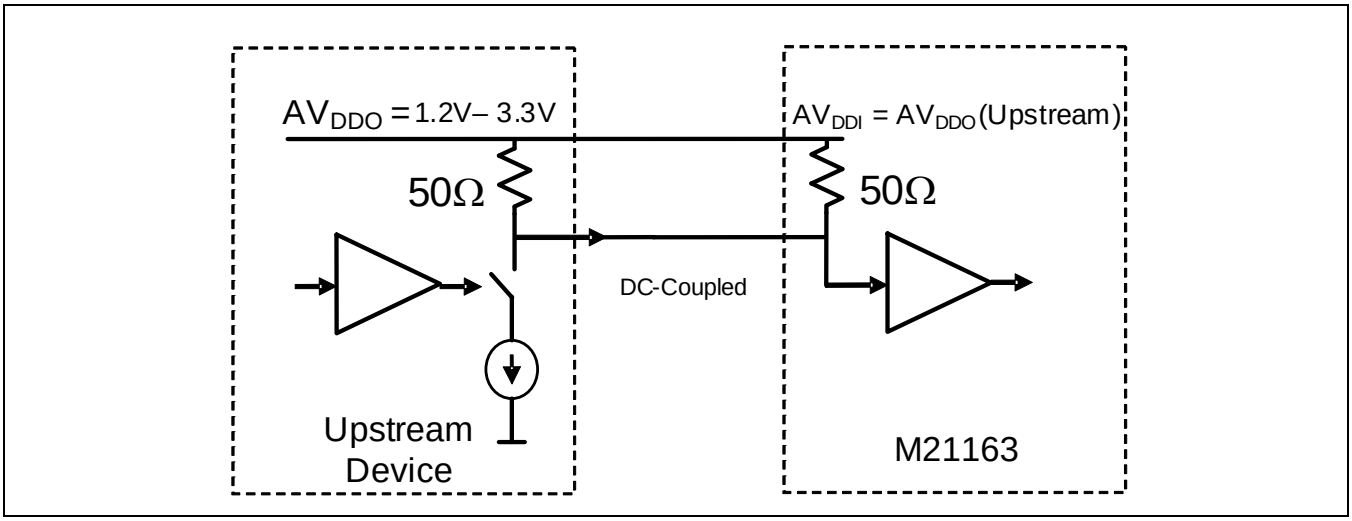
4.2 Reconfigurable Buffers Set as Input Ports

The 24 high-speed input lanes of the M21163 are designed to support both DC and AC coupled interfaces with external capacitors. After any power up and/or hardware/software reset, all input lanes are disabled. An input buffer "M" may be individually enabled or powered-down, by programming register.**InCtrl(M)**bit[4]; register address 80h through 91h.

NOTE: A reconfigurable buffer can be set to be either an input port or an output port, but not both at the same time.

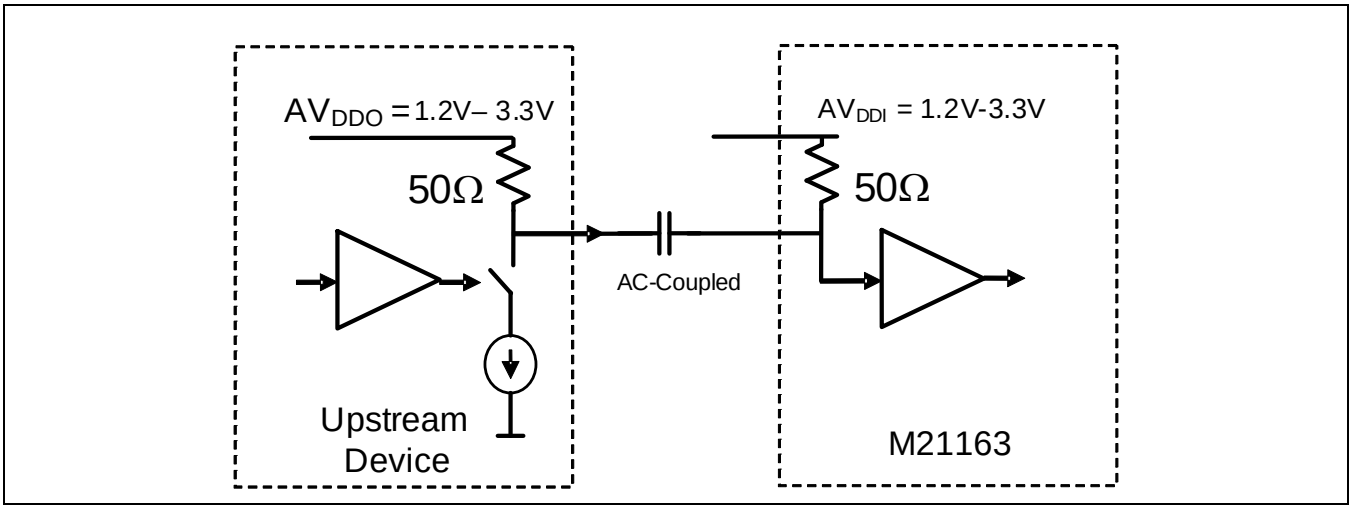
In order to accommodate DC coupling with the upstream device, each pin.**AV_{DDIO}**[23:0] power domain of the M21163 is electrically independent from all other power domains, therefore allowing it to be tied to the AV_{DDO} of the upstream device. For correct operation in DC coupled applications the input common mode voltage should match the output common mode voltage set by the transmitting devices driving the M21163.

Figure 4-2. DC-Coupling the Input of M21163



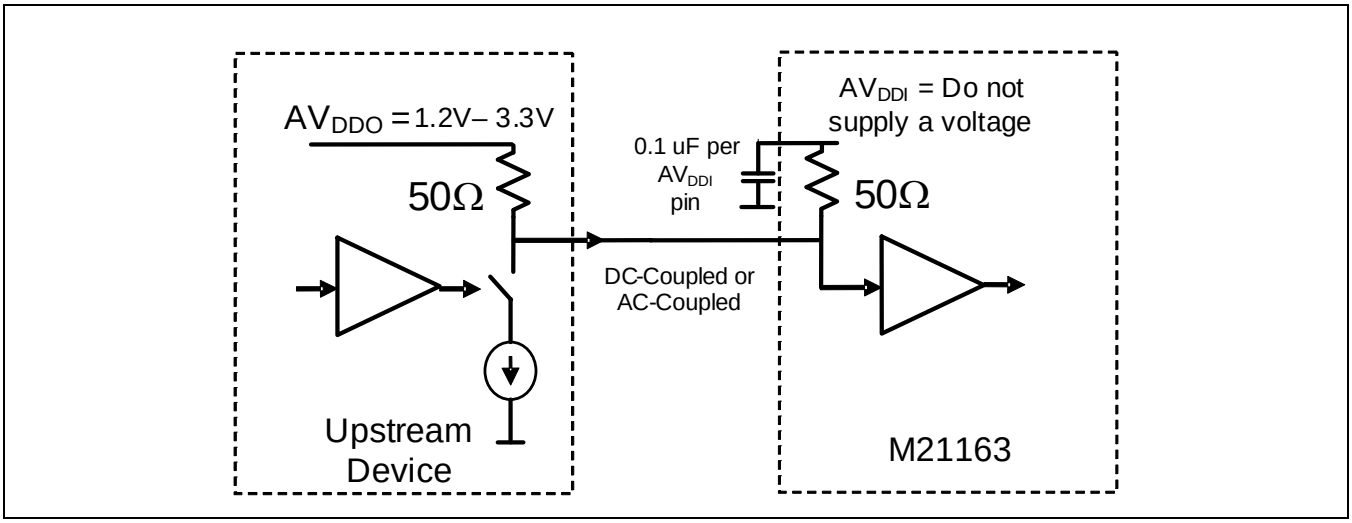
In most SDI applications, it is important to avoid AC coupled data interfaces between devices wherever possible. In addition to reducing the number of components, DC coupling will result in more system jitter margin. For AC coupled configurations, the recommended coupling capacitor is 10 µF for any Serial Digital Interface (SDI) video applications.

Figure 4-3. AC Coupling the Input of M21163



Alternatively the M21163 allows for the inputs to be self biased, eliminating the need for an electrical connection between the supply voltages of the upstream device and M21163. This configuration offers the benefit of keeping the supply of the previous device and the power domain(s) of the M21163 completely isolated.

Figure 4-4. Self Biasing the Input of the M21163



Note:
1. For self-bias applications, AV_{DDI} is not to be supplied with any voltage level. The common mode voltage will be generated internally. Please add a 0.1 µF capacitor per AV_{DDI} pin as shown in Figure 4-4.

4.2.1 Input Equalization

Each input lane is equipped with configurable equalization to compensate for the losses that a high-speed signal accumulates after transmission across long copper traces. Input equalization can be configured on a per lane basis and there are eight levels provided, from 0 dB to 6 dB maximum. Individual equalization control for lane "M" may be achieved by setting register.**InCtrl(M)**.bits[2:0] to the desired value.

4.2.2 DCD Correction Loop

All input lanes also feature an automatic offset correction loop to help compensate for DCD (Duty Cycle Distortion) or DC offset. The correction loop is designed to support the video pathological line event seen in SDI applications. For best performance, Mindspeed recommends leaving this feature enabled unless some testing or debug is required or when data rates of 143 Mbps or below are used; then the DCD correction loop must be disabled. The offset correction loop for an input lane "M" can be configured by setting register.**InCtrl**.bit[5] to the desired value.

4.2.3 Input Buffer Polarity Flip

Each input lane can have its polarity flipped to ease board routing. The polarity is controlled per lane via register.**InCtrl**.bit[3], where "0b" is normal polarity and "1b" is inverted polarity. Note that there is also independent polarity flip associated with each output lane as described in Section 4.3. Having independent polarity flip allows the board designer complete polarity flexibility regardless of crosspoint configuration.

4.2.4 Input LOS Detection Circuitry

The M21163 features a Loss of Signal (LOS) detection circuitry on each input lane. The LOS threshold level for an input lane "M" can be configured individually by setting register.**InLos(M)**.bit[2:0]. The LOS detector threshold range can be set from 70 mV_{PPD} to 130 mV_{PPD} in 10 mV_{PPD} steps. If data rates below 143 Mbps are used, it is recommended to disable the LOS circuitry as low data rate signals can falsely trigger an LOS Alarm.

The LOS status of an input lane "M" can be read using register.**InLos(M)**.bit[7]. This bit will be a "1b" upon a LOS event. In addition to the LOS status, the M21163 has the capability to monitor changes on the LOS status register via the LOS alarm, register.**InLos(M)**.bit[6]. When the LOS alarm senses a change on the LOS status, bit[6] will be "1b". Writing a "1b" to register.**InLos(M)**.bit[6] will clear it.

At power-up or after any hardware/software reset, the logical OR of all the values in the LOS_alarm bits, register.**InLos(M)**.bit[6], can be monitored on hardware pin.**xALARM**. Alternatively, register.**InLos(M)**.bit[5] can be used to mask the LOS alarm coming from any unwanted channel.

Finally, LOS can be forced globally by using register.**GenConfig**.bit[4].

4.3 Reconfigurable Buffers Set as Output Ports and Dedicated Output Ports

The 32 high-speed output lanes of the M21163 are designed to be AC coupled, using external coupling capacitors, or DC coupled. All output pins have a single ended, on-device 50 Ω termination connected to pin.**AV_{DDO}**. An output buffer "M" may be individually enabled or powered down, by programming register.**OutCrtl(M)**bit[4]; register address A0h through BFh.

NOTE: A reconfigurable buffer can be set to be either an input port or an output port, but not both at the same time.

DC coupled operation can be supported but may change the common mode output voltage and differential output swing depending on the input circuitry of the downstream device. All of the figures (output swing and de-emphasis, power at pin.**AV_{DDO}**, etc.) in this document only apply to AC coupled outputs. The recommended coupling capacitor is at least 10 µF for any SDI video applications. Each output buffer is biased using the corresponding pin.**AV_{DDIO}** or pin.**AV_{DDO}**.

The differential output swing for an output "M" can be set to any of the three nominal settings of minimum, intermediate, and maximum by programming register.**OutCtrl(M)**.bit[5:4].

The M21163 also has a three-step (approximately 2 dB per step, 6 dB maximum), output de-emphasis capability. The output de-emphasis for an output "M" can be set by programming register.**OutCtrl(M)**.bit[1:0].

Additional features for a differential output "M" buffer such as power down, mute and polarity can be controlled by programming register.**OutCtrl(M)** bits 6, 3 and 2 respectively.

While the M21163 provides ultimate flexibility for configuring the input/output ports, output swing, and supply voltages, it is important to consider the heat dissipation and power consumption of the device when choosing the configuration. Mindspeed recommends that for configurations where the number of outputs greatly exceeds the number of inputs, lower AV_{DDO} supply voltages, or output swings be used. Configuring the M21163 with 1 input, 31 outputs, while setting AV_{DDO} to 3.3 V and output swing to max is not recommended.

4.4 Active Switch Configuration (ASC) Register

The M21163 features a fully non-blocking 32 port switching matrix. After power-up or any hardware/software reset, resister.**ASC(M)** will default to a non-valid configuration (FFh) and therefore each crosspoint lane is powered down.

There are three methods of changing and/or updating the switching matrix configuration:

- The direct ASC mode by programming the desired switching path registers.
- The hardware strobe mode, using pin.**xSET** and selectively loading one of two switching maps. The switching maps are stored on the Intermediate Switch Configuration registers (ISC1 and ISC2).

- The software strobe mode, using register.**Strobe**.bit[5:0] and selectively loading one of two pre-determined switching maps.

4.4.1 Direct ASC Mode

In this mode, any input lane can be independently and asynchronously routed to a specific output lane "M". Upon a direct write to the appropriate register.**ASC(M)** the new ASC register contents and the new switching configuration map will be immediately asserted, without requiring a hardware or software strobe event.

Direct ASC example: Route input13 to output0

Operation	Register	Data	Comment
Read	20h	1Fh	register.**ASC**(0). Default value for DIO0
Write	20h	0Dh	register.**ASC**(0). Route Output 0 to Input 13.

4.4.2 Hardware Strobe Mode

The M21163 features an external, switch configuration strobe input at hardware pin.**xSET**. The hardware strobe pins may be used to synchronously trigger updating the active switch configuration register. This is also the default switching mode after any power-up and/or hardware/software reset.

The active switching matrix configuration (ASC) may be loaded from either of the two configuration registers ISC1 and ISC2 upon a hardware strobe.

Upon power-up, hardware, or software reset, pin.**xSet** is used for both strobing and selecting which ISC register is loaded into the ASC register. A logic low on pin.**xSet** selects ISC1, and a logic high on pin.**xSet** selects ISC2. Therefore, a low-to-high transition on pin.**xSet** will load ISC1 into ASC since ISC1 was selected before the edge occurred. Conversely, a high-to-low transition on pin.**xSet** will load ISC2 into ASC.

Hardware Strobe/Selection Mode Example: Route input12/input13 to output0 using ISC1/ISC2.

Operation	Register	Data	Comment
Read	20h	1Fh	Default value for Channel 0 register.**ASC**
Write	40h	0Ch	Prepare to route Input 12 to Output 0 using register.**ISC1**
Write	60h	0Dh	Prepare to route Input 13 to Output 0 using register.**ISC2**
Low-to-High Transition on pin.**xSet**			
Read	20h	0Ch	Contents of register.**ISC1** were transferred to register.**ASC**
High-to-Low Transition on pin.**xSet**			
Read	20h	0Dh	Contents of register.**ISC2** were transferred to register.**ASC**

By programming register.**Strobe**.bit[6] to "1b", the user can change to software ISC selection control. In this mode, the falling edge of pin.**xSet** is used for strobing the ISC registers into ASC, but the selection is done by programming register.**Strobe**.bit[7]. Writing a "0b" will cause ISC1 to be selected on the next falling edge of pin.**xSet** and writing a "1b" will cause ISC2 to be selected on the next falling edge of pin.**xSet**.

Hardware Strobe/ Software Selection Mode Example: Route input12/input13 to output0 using ISC1/ISC2.

==========

Operation	Register	Data	Comment
Read	20h	1Fh	Default value for Channel 0 register.**ASC**
Write	01h	40h	Use software ISC selection and select ISC1
Write	40h	0Ch	Prepare to route Input 12 to Output 0 using register.**ISC1**
Write	60h	0Dh	Prepare to route Input 13 to Output 0 using register.**ISC2**
High-to-Low Transition on pin.**xSet**			
Read	20h	0Ch	Contents of register.**ISC1** were transferred to register.**ASC**
Write	01h	C0h	Use software ISC selection and select ISC2
High-to-Low Transition on pin.**xSet**			
Read	20h	0Dh	Contents of register.**ISC2** were transferred to register.**ASC**

4.4.3 Software Strobe Mode

The M21163 features an internal, switch configuration strobe input using register.**Strobe**.bit[5:0]. The software strobe may be used to synchronously trigger updating the active switch configuration register. After any power-up and/or hardware/software reset, the hardware strobe mode is selected. To change the device to Software Strobe Mode, the user must write a "0b" to register.**GenConfig**.bit[7]. Note that the pin.**xSet** is not used in software strobe mode.

Software Strobe Mode Example: Route input12/input13 to output0 using ISC1/ISC2.

==========

Operation	Register	Data	Comment
Read	20h	1Fh	Default value for Channel 0 register.**ASC**
Write	00h	00h	Selects Software Strobe Mode on register.**GenConfig**
Write	40h	0Ch	Prepare to route Input 12 to Output 0 using register.**ISC1**
Write	60h	0Dh	Prepare to route Input 13 to Output 0 using register.**ISC2**
Write	01h	00h	Select ISC1
Write	01h	15h	Execute software strobe
Write	01h	00h	Software strobe back to normal operation
Read	20h	0Dh	Contents of register.**ISC1** were transferred to register.**ASC**
Write	01h	80h	Select ISC2
Write	01h	95h	Execute software strobe
Write	01h	00h	Software strobe back to normal operation
Read	20h	0Ch	Contents of register.**ISC2** were transferred to register.**ASC**

4.5 Temperature Monitoring

The M21163 features four embedded, integrated temperature sensors, one at each corner of the die. Each sensor has an effective range from approximately -45 °C to +135 °C, stepped in 10 °C increments. The sensors can be configured using register.**TempMonCtrl**.

The device temperature sensors are enabled after power up or any hardware/software reset. They can be disabled by programming register.**TempMonCtrl**.bit[1] to "0b".

The readings for the temperature sensors located in the top-right and top-left corners of the die are available in register.**TempMonT**. Similarly, the readings from temperature sensors in the bottom-right and bottom-left corners of the die are available in register.**TempMonB**. A user provided digital strobe is required to load the temperature values into the two registers. This is accomplished by issuing a rising edge on the strobe signal located at register.**TempMonCtrl**.bit[0].

Sensor configuration allows for activating an alarm at pin.**xAlarm** to indicate when the device temperature has exceeded a certain level as detected by the top right temperature sensor. By default, the alarm is activated and set to active low. Triggering the pin.**xALARM** due to over temperature can be disabled by programming register.**TempMonCtrl**.bit[7] to "1b".

The temperature threshold for asserting the alarm can be set to a value between 50 °C to 135 °C by programming register.**TempMonCtrl**.bit[4:2]. Note that the device can sustain permanent damage at a temperature of 130 °C and setting the alarm to that threshold is not recommended.

The M21163 temperature alarm can be configured to latch the over-temperature alarm by writing "1b" to register.**OvertempLatch**.bit[1]. In this mode, the alarm remains high after the temperature exceeds the programmed threshold, and can be cleared only by writing "1b" to register.**OvertempLatch**.bit[1]. This clearing bit should be written back to "0b" for normal operation.

4.6 Software Interfaces

The registers of the M21163 can be configured through two different control interfaces:

- Two-wire serial interface operational at the standard data rates of 100 kHz, 400 kHz, and 3.4 MHz.
- Four-wire serial interface operational up to 100 MHz for register writes and up to 25 MHz for register reads.

In addition to the control interfaces, the M21163 may be set to support JTAG.

The digital control mode is determined by setting pin.**MF**[1:0] as shown in Table 4-1 below.

Table 4-1. Digital Control Mode

MF[1:0]	Description
LL	Four-wire digital interface selected
LH	JTAG digital interface selected
HL	Two-wire digital interface selected
HH	Unused

4.6.1 Two-Wire (I^2C) Digital Interface

In this mode, a two-wire serial interface is used to program the device's internal registers, configuring the operation of the M21163. When in two-wire mode, MF[5:2] pins comprise the two-wire bus as shown in Table 4-2 below.

Table 4-2. MF Pin Configuration in Two-Wire Digital Interface Mode

MF Pin	Two-Wire Pin Name	Function
MF2	ADD0	Address bit 0
MF3	ADD1	Address bit 1
MF4	SDA	Serial Data Input/Output
MF5	SCL	Serial Clock Input from Master Host

The M21163 allows for nine different addresses to be programmed using the inputs ADD[1:0]; these inputs have three states, low (L), high (H) and floating (F). The slave addresses are from 20h to 28h.

Table 4-3. Two-Wire Digital Interface Address

I^2C Addr1 (MF3)	I^2C Addr0 (MF2)	I^2C Address (Binary)	I^2C Address (Hexadecimal)
L	L	0010 0000b	20h
L	H	0010 0001b	21h
H	L	0010 0010b	22h
H	H	0010 0011b	23h
L	F	0010 0100b	24h
H	F	0010 0101b	25h
F	L	0010 0110b	26h
F	H	0010 0111b	27h
F	F	0010 1000b	28h

Figure 4-5 illustrates typical waveforms and timing seen at SCL and SDA for a read and write operation.

Figure 4-5. Two-wire Timing

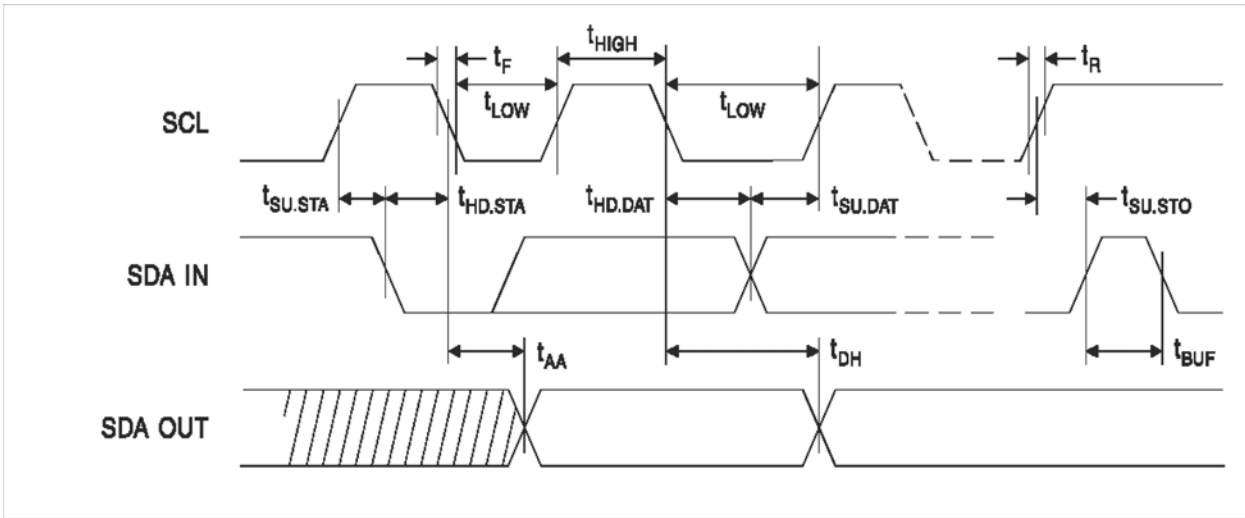


Table 4-4. Two-wire Slave Timing Specifications (Standard Mode or Fast Mode)

Symbol	Parameter	Min	Typ	Max	Units
f_{SCL}	Clock Frequency, SCL	–	–	400	kHz
t_{LOW}	Clock Pulse Width Low	1.3	–	–	µs
t_{HIGH}	Clock Pulse Width High	1	–	–	µs
t_{AA}	Clock Low to Data Out Valid	0.05	–	0.9	µs
t_{HDSTA}	Start Hold Time	200	–	–	ns
t_{SUSTA}	Start Set-up Time	200	–	–	ns
t_{HDDAT}	Data In Hold Time	0	–	–	ns
t_{SUDAT}	Data In Set-up Time	100	–	–	ns
t_{SUSTO}	Stop Set-up Time	200	–	–	ns
t_{DH}	Data Out Hold Time	50	–	–	ns

Table 4-5. Two-wire Slave Timing Specifications (High Speed Mode)

Symbol	Parameter	Min	Typ	Max	Units
f_{SCL}	Clock Frequency, SCL	–	–	3.4	MHz
t_{LOW}	Clock Pulse Width Low	160	–	–	ns
t_{HIGH}	Clock Pulse Width High	60	–	–	ns
t_{AA}	Clock Low to Data Out Valid	0	–	70	ns
t_{HDSTA}	Start (repeated) Hold Time	160	–	–	ns
t_{SUSTA}	Start (repeated) Set-up Time	160	–	–	ns
t_{HDDAT}	Data In Hold Time	0	–	–	ns
t_{SUDAT}	Data In Set-up Time	10	–	–	ns
t_{SUSTO}	Stop Set-up Time	160	–	–	ns
t_{DH}	Data Out Hold Time	5	–	–	ns
Notes: Max CAP load for SDA is 100 pF.					

4.6.2 Four-Wire Digital Interface

In this mode, a four-wire serial interface is used to program the device's internal registers, configuring the operation of the M21163. When in four-wire mode, MF[5:2] pins comprise the four-wire bus as shown in Table 4-6 below.

Table 4-6. MF Pin Configuration in Four-wire Interface Mode

MF Pin	Four-wire Pin Name	Function
MF2	xCS	Chip Select (Active Low)
MF3	SI	Serial Data Input
MF4	SO	Serial Data Output
MF5	SCLK	Serial Clock Input

The interface shifts data in from the external controller on the rising edge of SCLK. The serial I/O operation is gated by xCS. Data is shifted in to M21163 from the Host (Master) to SI on the falling edge of SCLK, and shifted out through SO on the rising edge of SCLK. To address a register, a 10-bit input needs to be shifted, consisting of the first bit (Start Bit, SB = 1), the second bit (Operation Bit, OP = 1 for read, = 0 for write), and the 8-bit address (MSB first).

Figure 4-6. Four-wire Interface Word Format

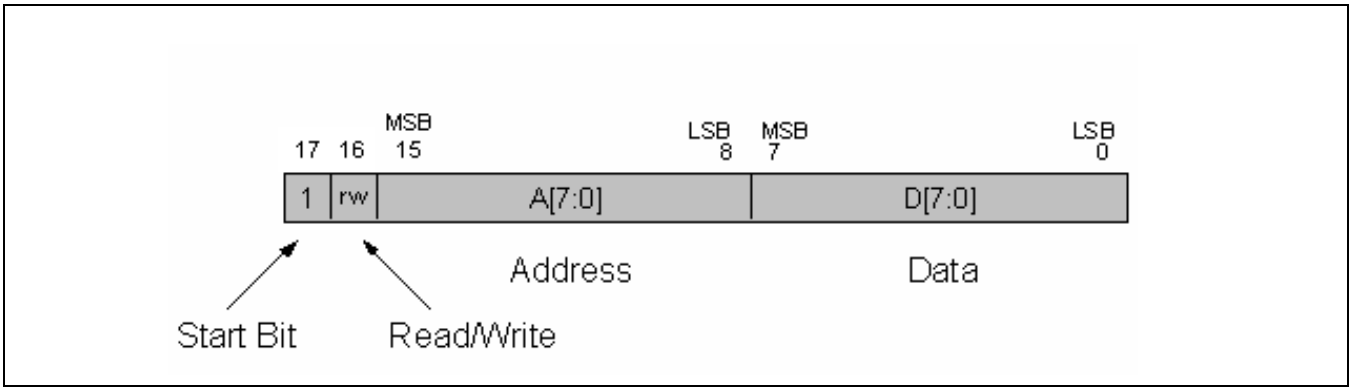
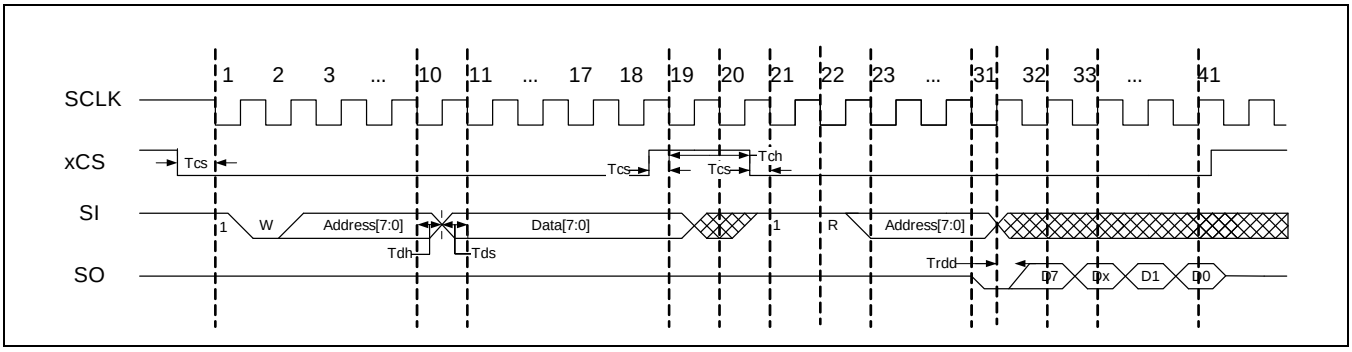


Figure 4-7 illustrates a Serial Write Mode followed by a Serial Read mode. To initiate a Write sequence, xCS goes low before the falling edge of SCLK. On each falling edge of the clock, the 18 bits consisting of the SB = 1, OP = 0, ADDR, and DATA, are latched into the input shift register through SI. The rising edge of xCS may occur before or after the falling edge of SCLK for the last bit. Upon receipt of the last bit, one additional cycle of SCLK is necessary before DATA transfers from the input shift register to the addressed register.

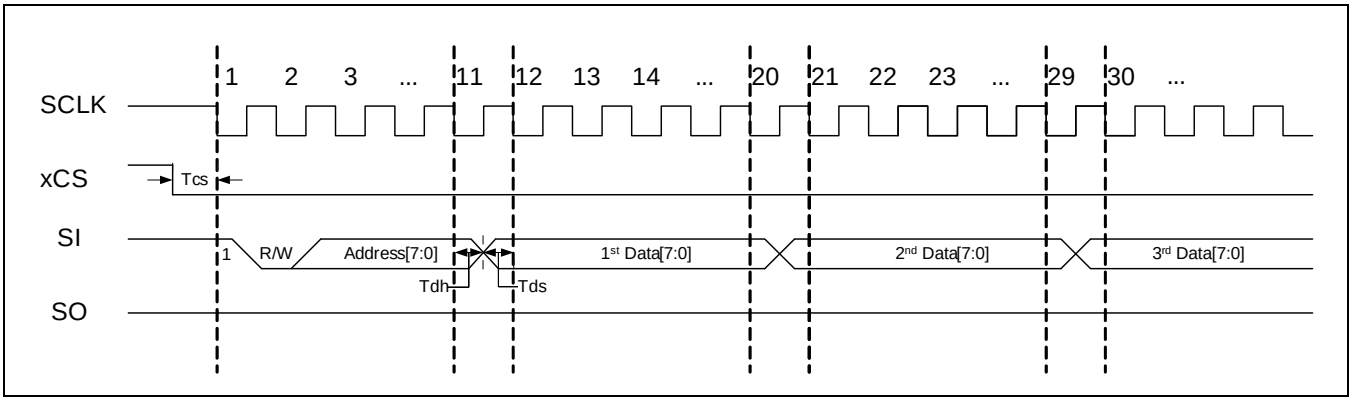
To initiate a read sequence, xCS goes low before the falling edge of SCLK. On each falling edge of SCLK, the 10 bits consisting of SB = 1, OP = 1, and the 8-bit ADDR are written to the serial input shift register and copied to the serial output shift register. On the next rising edge after the address LSB, the SB and 8 bits of the DATA are shifted out. The SB for a Read is always 1.

Figure 4-7. Four-Wire Write Followed by a Read Sequence



The 4-wire interface supports multiple consecutive writes. In this case, the address header is not needed and each additional 8 bits of data will be written into consecutive addresses. If consecutive read/write cycles are being performed, it is not necessary to insert an extra clock cycle between read/write cycles, however one extra clock cycle is needed after the last data bit of the last read/write cycle.

Figure 4-8. Four-Wire Sequential WRITE



On a Write cycle, any bits that follow the expected number of bits are ignored, and only the first 15 bits following SB and OP are used. On a Read cycle, any extra clock cycles will result in the repeat of the data LSB. An invalid SB or OP renders the operation undefined. The falling edge of xCS always resets the serial operation for a new Read or Write cycle.

Detailed timing information is shown below.

Table 4-7. Four-wire Interface Timing

Timing Symbol	Description	Min	Max	Unit
Tds	Data set-up time	2.5	—	ns
Tdh	Data hold time	2.5	—	ns
Tcs	xCS set-up time	2.5	—	ns
Tch	xCS hold time	2.5	—	ns
Tfreq, write	Four-wire interface write clock frequency	—	100	MHz
Tfreq, read	Four-wire interface read clock frequency DV_{DDIO}=1.2 V, 1.8 V Maximum load capacitance 10 pF	—	25	MHz
	Four-wire interface read clock frequency DV_{DDIO}=2.5 V, 3.3 V Maximum load capacitance 30 pF	—	50	MHz
T_{DUTY}	SCLK duty cycle	40	60	%
Tdd	Four-wire interface read data output delay DV_{DDIO}=1.2 V, 1.8 V Maximum load capacitance 10 pF	2	17	ns
	Four-wire interface read data output delay DV_{DDIO}=2.5 V, 3.3 V Maximum load capacitance 30 pF	2	9	ns

4.6.3 JTAG Interface Mode

The M21163 may be set to JTAG mode to perform boundary scan. This mode is enabled by setting pin.MF[1:0] to "01b". The standard interface pins TDI, TMS, TCLK, TDO are mapped to MF pins as shown in Table 4-8 below.

All of the reconfigurable I/O on the M21163 are implemented as bi-directional scan cells. The scan pattern should be created appropriately considering the actual directionality of the I/Os as used on the board. When JTAG mode is enabled, the M21163 automatically bypasses the software registers enabling all dedicated output drivers. The JTAG boundary scan includes all 32 channels.

When in JTAG Mode, MF[6:2] pins comprise the bus as shown in Table 4-8 below.

Table 4-8. MF Pin Configuration in JTAG Interface Mode

MF Pin	JTAG Pin Name	Function
MF2	TDI	Test Data In
MF3	—	Not used
MF4	TMS	Test Mode State
MF5	TCLK	Test Clock
MF6	TDO	Test Data Out

5.0 Control Registers Map and Descriptions

5.1 Control Registers Map

Table 5-1. Register Summary

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
00h	GenConfig	strobe_ctrl	MSPD Reserved	pd_gbl	force_los	MSPD Reserved	force_in_on	MSPD Reserved		80'h	R/W
01h	Strobe	isc_sel	isc_sel_ctrl	set						00'h	R/W
02h	TempMonCtrl	dis_xalarm_ot	unused	xalarm_ot_pol	jtemp_thr			en_temp_mon	strobe_temp	12'h	R/W
03h	OvertempLatch	MSPD Reserved						alarm_latch_en	clear_alarm	00'h	R/W
04h	Reserved	MSPD Reserved								00'h	R/W
20h-3Fh	ASC	MSPD Reserved			ASCout					1F'h	R/W
40h-5Fh	ISC1	MSPD Reserved			ISC1out					1F'h	R/W
60h-77h	ISC2	MSPD Reserved			ISC2out					1F'h	R/W
80h-97h	InCtrl	MSPD Reserved		pd_dcoff_in	cfg_in	polflip_in	ie_ctrl			00'h	R/W
A0h-BFh	OutCtrl	MSPD Reserved	cfg_out	outlvl		domute	polflip_out	de		A0'h	R/W
C0h-D7h	InLos	los_status	los_alarm	los_mask	never_sq	sq_pol_low	los_vthr			01'h	R/W
E0h	MasterRst	reset								00'h	R/W
E1h	ChipCode	chipcode								13'h	R
E2h	RevCode	revcode								00'h	R
E3h	TempMonT	tempTL				tempTR				NA	R
E4h	TempMonB	tempBL				tempBR				NA	R

5.2 Control Registers Descriptions

Address: 00h
Register Name: GenConfig
Default Value: 80'h
Description: General Configuration Register.

Bit	Name	Description	Default	Type
7	strobe_ctrl	0b: Switch setting change with software Strobe[5:0] registers 1b: Switch setting changed with hardware pin.**xSET**	1b	R/W
6	Reserved	Reserved	0b	R/W
5	pd_gbl	0b: Normal operation 1b: Global powerdown	0b	R/W
4	force_los	0b: Normal operation 1b: Force LOS alarm to be activated (globally applied for all input channels)	0b	R/W
3	Reserved	Reserved	0b	R/W
2	force_in_on	0b: Input powerdown is controlled by XPT settings 1b: Force input channel on	0b	R/W
[1:0]	Reserved	Reserved	00b	R/W

Address: 01h
Register Name: Strobe
Default Value: 00'h
Description: XPT address strobe control

Bit	Name	Description	Default	Type
7	isc_sel	0b: Selects ISC1 as the active state to become ASC upon strobe (register.**GenConfig**.bit[7]=0 or register.**GenConfig**.bit[7]/register.**Strobe**.bit[6]=11) 1b: Selects ISC2 as the active state to become ASC upon strobe (register.**GenConfig**.bit[7]=0 or register.**GenConfig**.bit[7]/register.**Strobe**.bit[6]=11)	0b	R/W
6	isc_sel_ctrl	0b: Pin.**xSET** selects which ISC to latch upon strobe (register.**GenConfig**.bit[7]=1) 1b: register.**Strobe**.bit[7] selects which ISC to latch upon strobe (register.**GenConfig**.bit[7]=1)	0b	R/W
[5:0]	set	000000b: Normal operation 010101b: Register strobe causes ISC1 or ISC2 to become ASC, changing the switch state (when register.**GenConfig**.bit[7]=0b)	000000b	R/W

Address: 02h
Register Name: TempMonCtrl
Default Value: 12'h
Description: Temperature monitor control

Bit	Name	Description	Default	Type
7	dis_xalarm_ot	0b: pin.**xAlarm** on overtemp active 1b: pin.**xAlarm** on overtemp disabled	0b	R/W
6	Reserved	Reserved	0b	R/W
5	xalarm_ot_pol	0b: pin.**xAlarm** is set to low whenever T_{JUNC} exceeds the threshold as defined at bit[4:2] 1b: pin.**xAlarm** is set to high whenever T_{JUNC} exceeds the threshold as defined at bit[4:2]	0b	R/W
[4:2]	jtemp_thr	Junction temperature alarm threshold 000b: 50 °C 001b: 65 °C 010b: 82.5 °C 011b: 97.5 °C 100b: 115 °C 101b: 120 °C 110b: 130 °C 111b: 135 °C	100b	R/W
1	en_temp_mon	0b: Disable temperature monitor 1b: Enable and power up the temperature monitor	1b	R/W
0	strobe_temp	Strobes ADC for temperature measurement. 0b: Ready to read temperature 1b: Read temperature (Note 1)	0b	R/W

NOTES:
1. User should strobe temp by writing 1b followed by 0b before reading the temperature.

Address: 03h
Register Name: OvertempLatch
Default Value: 00'h
Description: Overtemp latch control

Bit	Name	Description	Default	Type
[7:2]	Reserved	Reserved	000000b	R/W
1	alarm_latch_en	0b: Overtemp latch function disabled 1b: Overtemp latch function enabled	0b	R/W
0	clear_alarm	0b: Normal operation 1b: To clear the alarm at pin xAlarm, write 1b then write 0b back	0b	R/W

Address: 04h
Register Name: MSPD Reserved
Default Value: 00'h
Description: MSPD Reserved

Bit	Name	Description	Default	Type
[7:0]	Reserved	Reserved	00000000b	R/W

Address: HEX(32 + n) n=0...31
20h 21h 22h 23h 24h 25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh 30h 31h 32h 33h 34h 35h 36h 37h 38h 39h 3Ah 3Bh 3Ch 3Dh 3Eh 3Fh
Register Name: ASC
Default Value: 1F'h
Description: ASC contains the current switch state. Writing to this register will cause the switch state to change immediately in an asynchronous manner.

Bit	Name	Description	Default	Type
[7:5]	Reserved	Reserved	000b	R
[4:0]	ASCout	00000b: Route input lane 0 to output lane M 00001b: Route input lane 1 to output lane M 0000000b: ... 10111b: Route input lane 23 to output lane M	11111b	R/W

Address: HEX(64 + n) n=0...31
40h 41h 42h 43h 44h 45h 46h 47h 48h 49h 4Ah 4Bh 4Ch 4Dh 4Eh 4Fh 50h 51h 52h 53h 54h 55h 56h 57h 58h 59h 5Ah 5Bh 5Ch 5Dh 5Eh 5Fh
Register Name: SC1
Default Value: 1F'h
Description: ISC1 contains one of two possible next switch states that can become the current state through the strobe function.

Bit	Name	Description	Default	Type
[7:5]	Reserved	Reserved	000b	R
[4:0]	ISC1out	00000b: Route input lane 0 to output lane M 00001b: Route input lane 1 to output lane M 0000000b: ... 10111b: Route input lane 23 to output lane M	11111b	R/W

Address: HEX(96 + n) n=0...31
60h 61h 62h 63h 64h 65h 66h 67h 68h 69h 6Ah 6Bh 6Ch 6Dh 6Eh 6Fh 70h 71h 72h 73h 74h 75h 76h 77h 78h 79h 7Ah 7Bh 7Ch 7Dh 7Eh 7Fh
Register Name: ISC2
Default Value: 1F'h
Description: ISC2 contains one of two possible next switch states that can become the current state through the strobe function.

Bit	Name	Description	Default	Type
[7:5]	Reserved	Reserved	000b	R
[4:0]	ISC2out	00000b: Route input lane 0 to output lane M 00001b: Route input lane 1 to output lane M 0000000b: ... 10111b: Route input lane 23 to output lane M	11111b	R/W

Address: HEX(128 + n) n=0...23
80h 81h 82h 83h 84h 85h 86h 87h 88h 89h 8Ah 8Bh 8Ch 8Dh 8Eh 8Fh 90h 91h 92h 93h 94h 95h 96h 97h
Register Name: InCtrl(M)
Default Value: 00'h
Description: Input configuration registers.

Bit	Name	Description	Default	Type
[7:6]	Reserved	Reserved	00b	R
5	pd_dcoff_in	0b: Input DC offset correction on 1b: Input DC offset correction off	0b	R/W
4	cfg_in	0b: Input powered off 1b: Input powered on	0b	R/W
3	polflip_in	0b: Input side polarity normal 1b: Input side polarity flipped	0b	R/W
[2:0]	ie_ctrl	000b: Min EQ boost (0 dB) ... 111b: Max EQ boost (6 dB)	000b	R/W

Address: HEX(160 + n) n=0...31
A0h A1h A2h A3h A4h A5h A6h A7h A8h A9h AAh ABh ACh ADh AEh AFh B0h B1h B2h B3h B4h B5h B6h B7h B8h B9h BAh BBh BCh BDh BEh BFh
Register Name: OutCtrl(M)
Default Value: A0'h
Description: Output configuration registers.

Bit	Name	Description	Default	Type
7	Reserved	Reserved	1b	R/W
6	cfg_out	0b: Output powered off 1b: Output powered on (Note 1)	0b	R/W
[5:4]	outlvl	00b: Output powered off 01b: 600 mV_{PPD} output swing 10b: 800 mV_{PPD} output swing 11b: 1200 mV_{PPD} output swing	10b	R/W
3	domute	0b: Do not mute the output 1b: Mute the output	0b	R/W
2	polflip_out	0b: Output side polarity normal 1b: Output side polarity flipped	0b	R/W
[1:0]	de	00b: Output de-emphasis disabled 01b: Lowest de-emphasis setting 10b: Medium de-emphasis setting 11b: Highest de-emphasis setting	00b	R/W

NOTES:
1. Output will not turn on when the input is on.

Address: HEX(192 + n) n=0...23
C0h C1h C2h C3h C4h C5h C6h C7h C8h C9h CAh CBh CCh CDh CEh CFh D0h D1h D2h D3h D4h D5h D6h D7h
Register Name: InLos(M)
Default Value: 01'h
Description: Input LOS control registers.

Bit	Name	Description	Default	Type
7	los_status	0b: Loss-of-signal not asserted 1b: Loss-of-signal asserted	0b	R
6	los_alarm	0b: Latched loss-of-signal not asserted 1b: Latched loss-of-signal asserted (Note 1)	0b	R/W
5	los_mask	0b: This lane's los_alarm is NOR'd with the other channels to create the xAlarm signal 1b: This lane's los_alarm is not NOR'd with the other channels to create the xAlarm signal	0b	R/W
4	never_sq	0b: Squelch this lane upon LOS alarm 1b: Do not squelch this lane upon LOS alarm	0b	R/W
3	sq_pol_low	0b: Squelch this lane to logic high state 1b: Squelch this lane to logic low state	0b	R/W
[2:0]	los_vthr	000b: 70 mV_{PPD} assert, 80 mV_{PPD} de-assert 001b: 80 mV_{PPD} assert, 90 mV_{PPD} de-assert 010b: 90 mV_{PPD} assert, 100 mV_{PPD} de-assert 011b: 100 mV_{PPD} assert, 110 mV_{PPD} de-assert 100b: 110 mV_{PPD} assert, 120 mV_{PPD} de-assert 101b: 120 mV_{PPD} assert, 130 mV_{PPD} de-assert 110b: 130 mV_{PPD} assert, 140 mV_{PPD} de-assert 111b: LOS power down	001b	R/W

NOTES:

1. Latched high on a transition in either direction of LOS signal. Clear by writing a 1.

Address: E0h
Register Name: MasterRst
Default Value: 00'h
Description: Global reset. Resets all registers to default value.

Bit	Name	Description	Default	Type
[7:0]	reset	00000000b: normal operation 10101010b: assert global reset	00000000b	R/W

Address: E1h
Register Name: ChipCode
Default Value: 13h
Description: Product identification code.

Bit	Name	Description	Default	Type
[7:0]	chipcode	Product identification code.	00010011b	R

Address: E2h
Register Name: RevCode
Default Value: 00h
Description: Product revision code

Bit	Name	Description	Default	Type
[7:0]	revcode	M21163-11	00000000b	R

Address: E3h
Register Name: TempMonT
Default Value: na
Description: Die top left and right temperature monitor readings.

Bit	Name	Description	Default	Type
[7:4]	tempTL	Die bottom left temperature reading 0000b: T_{JUNC} < -45 °C 0001b: range T_{JUNC} [-45 : -40] °C 0010b: range T_{JUNC} [-40 : -30] °C 0011b: range T_{JUNC} [-30 : -25] °C 0100b: range T_{JUNC} [-25 : -10] °C 0101b: range T_{JUNC} [-10 : 20] °C 0110b: range T_{JUNC} [20 : 35] °C 0111b: range T_{JUNC} [35 : 50] °C 1000b: range T_{JUNC} [50 : 65] °C 1001b: range T_{JUNC} [65 : 80] °C 1010b: range T_{JUNC} [80 : 95] °C 1011b: range T_{JUNC} [95 : 110] °C 1100b: range T_{JUNC} [110 : 115] °C 1101b: range T_{JUNC} [115 : 125] °C 1110b: range T_{JUNC} [125 : 130] °C 1111b: range T_{JUNC} > 130 °C		R
[3:0]	tempTR	Die top right temperature reading 0000b: T_{JUNC} < -45 °C 0001b: range T_{JUNC} [-45 : -40] °C 0010b: range T_{JUNC} [-40 : -30] °C 0011b: range T_{JUNC} [-30 : -25] °C 0100b: range T_{JUNC} [-25 : -10] °C 0101b: range T_{JUNC} [-10 : 20] °C 0110b: range T_{JUNC} [20 : 35] °C 0111b: range T_{JUNC} [35 : 50] °C 1000b: range T_{JUNC} [50 : 65] °C 1001b: range T_{JUNC} [65 : 80] °C 1010b: range T_{JUNC} [80 : 95] °C 1011b: range T_{JUNC} [95 : 110] °C 1100b: range T_{JUNC} [110 : 115] °C 1101b: range T_{JUNC} [115 : 125] °C 1110b: range T_{JUNC} [125 : 130] °C 1111b: range T_{JUNC} > 130 °C		R

NOTES:

1. Temperature values are approximate, and are NOT guaranteed.

Address: E4h
Register Name: TempMonB
Default Value: na
Description: Die bottom left and right temperature monitor readings.

Bit	Name	Description	Default	Type
[7:4]	tempBL	Die bottom left temperature reading 0000b: T_{JUNC} < -45 °C 0001b: range T_{JUNC} [-45 : -40] °C 0010b: range T_{JUNC} [-40 : -30] °C 0011b: range T_{JUNC} [-30 : -25] °C 0100b: range T_{JUNC} [-25 : -10] °C 0101b: range T_{JUNC} [-10 : 20] °C 0110b: range T_{JUNC} [20 : 35] °C 0111b: range T_{JUNC} [35 : 50] °C 1000b: range T_{JUNC} [50 : 65] °C 1001b: range T_{JUNC} [65 : 80] °C 1010b: range T_{JUNC} [80 : 95] °C 1011b: range T_{JUNC} [95 : 110] °C 1100b: range T_{JUNC} [110 : 115] °C 1101b: range T_{JUNC} [115 : 125] °C 1110b: range T_{JUNC} [125 : 130] °C 1111b: range T_{JUNC} > 130 °C		R
[3:0]	tempBR	Die bottom right temperature reading 0000b: T_{JUNC} < -45 °C 0001b: range T_{JUNC} [-45 : -40] °C 0010b: range T_{JUNC} [-40 : -30] °C 0011b: range T_{JUNC} [-30 : -25] °C 0100b: range T_{JUNC} [-25 : -10] °C 0101b: range T_{JUNC} [-10 : 20] °C 0110b: range T_{JUNC} [20 : 35] °C 0111b: range T_{JUNC} [35 : 50] °C 1000b: range T_{JUNC} [50 : 65] °C 1001b: range T_{JUNC} [65 : 80] °C 1010b: range T_{JUNC} [80 : 95] °C 1011b: range T_{JUNC} [95 : 110] °C 1100b: range T_{JUNC} [110 : 115] °C 1101b: range T_{JUNC} [115 : 125] °C 1110b: range T_{JUNC} [125 : 130] °C 1111b: range T_{JUNC} > 130 °C		R

NOTES:

1. Temperature values are approximate, and are NOT guaranteed.

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