

Advance Information

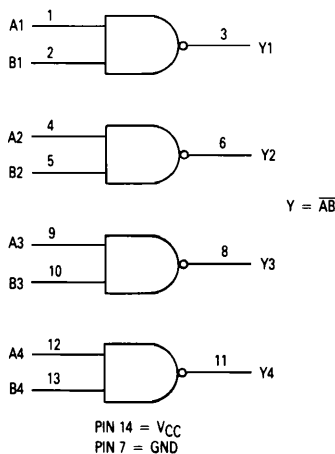
Quad 2-Input NAND Gate

High-Performance Silicon-Gate CMOS

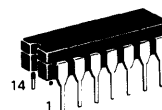
The MC54/74HC00A is identical in pinout to the LS00. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 32 FETs or 8 Equivalent Gates
- Improvements over HC00
 - Improved Propagation Delays
 - 50% Lower Quiescent Power
 - Improved Input Noise and Latchup Immunity

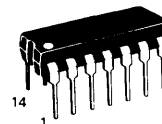
LOGIC DIAGRAM



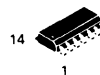
MC54/74HC00A



J SUFFIX
 CERAMIC
 CASE 632-08



N SUFFIX
 PLASTIC
 CASE 646-06



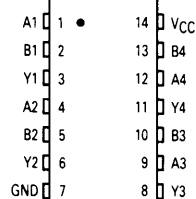
D SUFFIX
 SOIC
 CASE 751A-02

ORDERING INFORMATION

MC74HCXXAN Plastic
 MC54HCXXAJ Ceramic
 MC74HCXXAD SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 6.

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC54/74HC00A

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP SOIC Package	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.4 0.4	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	1.0	10	40	μA

MC54/74HC00A

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

CPD	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: P _D = C _{PD} V _{CC} ² f + I _{CC} V _{CC}	Typical @ 25°C, V _{CC} = 5.0 V	pF
		22	

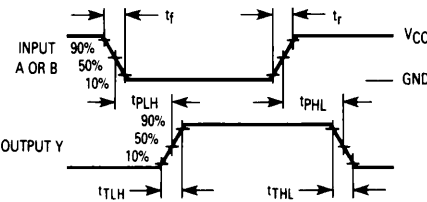
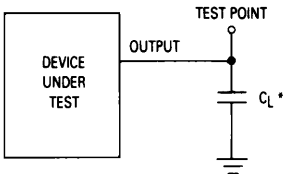


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

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EXPANDED LOGIC DIAGRAM
(1/4 of the Device)

